DTU Mechanical Engineering
Department of Mechanical Engineering

Implementation of Electrochemical Impedance Spectroscopy (EIS) for validation of humidity robustness of PCBA design elements

Simone Lauser

PhD Thesis

Technical University of Denmark

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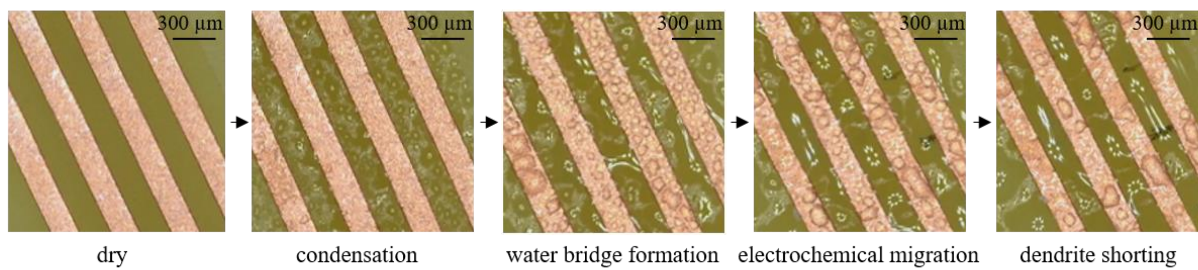

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PREFACE

The PhD project was supported by the Robert Bosch GmbH and CELCORR (Centre for Electronic Corrosion), DTU. The duration of the PhD program was from January 2018 to October 2020. The thesis is submitted in candidacy for a PhD degree from the Technical University of Denmark. The project entitled "Implementation of Electrochemical Impedance Spectroscopy (EIS) for validation of humidity robustness of PCBA design elements" has been carried out at the Department of Mechanical Engineering, Section of Materials and Surface Engineering, under the supervision of Professor Rajan Ambat and Dr. Vadimas Verdingovas and at Robert Bosch GmbH in Schwieberdingen, Germany, under the supervision of Dr. Theresia Richter.

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ABSTRACT

The motivation of this PhD project is the issue of climatic reliability testing of electronic devices with increasing complexity, with a focus on automotive electronics. Today's methods for assessing humidity and temperature induced failure modes are based on techniques that impose a DC potential to the Printed Circuit Board Assembly (PCBA) test specimen. While these approaches detect the occurrence of corrosive failures like dendritic growth due to electrochemical migration (ECM), they fail to distinguish the steps leading up to the failure. For evaluating the reliability of electronic assemblies, this impedes detailed knowledge on the cause-effect relationship of all influencing factors. The main focus of this work is to assess Electrochemical Impedance Spectroscopy (EIS) as an alternative non-destructive testing method, overcoming the drawbacks of DC testing. The primary purpose of the EIS approach is to trace the formation of a thin water layer on the surface of a PCBA. As EIS can distinguish between different resistive and capacitive processes, and states on the PCB under certain temperature and humidity conditions, water film formation can be monitored. This water film is the prerequisite for ECM to occur and the cause for various other moisture related PCBA failures and thus, understanding and controlling water film buildup can significantly improve the design for reliability already in the early stages of electronics development.

Chapter 1 provides an introduction into the topic of climatic reliability testing and scope of the work conducted within this PhD project. In chapter 2, the basics of automotive electronics development are summarized and the relevant humidity related aspects are covered. In addition, humidity related failure mechanisms in the PCBA context are described and the methodologies of climatic reliability testing are explained. Chapter 3 summarizes the literature review in the light of the purpose of the PhD project. Chapter 4 summarizes the materials and methods used as part of the different activities in the project. Various results from the research work are represented in the form of manuscripts, meant for publication in international journals. Chapter 5 summarizes each of the papers with the most important objectives and findings, before the complete papers are attached in the following chapters 6-9. In Paper 1, the water layer buildup on a PCB laminate surface is traced by EIS measurement and related to the occurrence of dendrite shorting upon using a DC based approach. In Paper 2, a measurement approach of alternating EIS and DC testing is used to provide a detailed allocation of sequential water layer buildup and Electrochemical Migration. Paper 3 deals with the localization of enhanced condensate formation on PCBA surfaces due to a temperature profile or the presence of contaminants. Impedance Spectroscopy and Time Domain Reflectometry are employed to assess the influence of these parameters. In Paper 4, an extensive evaluation of the EIS technique in terms of feasibility to determine climatic reliability is attempted. This includes a review of literature information as well as comprehensive evaluation of the results from Papers 1-3 and additional evaluation with the point of view of feasibility of using EIS as a complementary approach to DC

testing. Chapter 10 and Chapter 11 provide a general discussion and conclusion of the work and in Chapter 12; suggestions for future work are given.

Overall, the results from the investigations show the importance of appropriate climatic reliability testing methods. It was demonstrated that EIS as an alternative approach to the conventional DC-based SIR (Surface Insulation Resistance) method is a powerful method for assessing humidity robustness of PCBAs. The EIS method is not only non-destructive to the test specimen, but it was also shown that it can detect critical humidity states prior to signal changes in the DC. By comparing with the conventional SIR measurement approach, contrasting both methods clearly proved the general feasibility of using EIS as predictive tool for corrosion failures. A comprehensive understanding regarding the contribution of the PCBA design parameters, like surface properties and contamination impact, as well as climatic test conditions individually and combined could be obtained. It was shown that delivering a cause-effect relationship of the failure mode by EIS measurement and evaluation of resistive and capacitive system properties is possible. The condensation process and buildup of a water film and thus the prerequisite for corrosive processes like ECM can be determined by EIS threshold values without actually producing the failure. In this scope, a long time future investment in the EIS technique as a standardized method for PCBA humidity robustness evaluation is advisable.

DANSK RESUMÉ

Motivationen for dette ph.d.-projekt er at opnå en dybere forståelse af klimatiske påvirkninger på elektronik med fokus på elektronik til biler. Metoder til vurdering af fugt- og temperaturinducerede fejl af elektronik er ofte baseret på metoder, der benytter sig af et jævnstrømspotentiale ved test af printkort. Sådanne metoder vil vise forekomsten af fejl f.eks. forårsaget af elektrokemisk migration, men giver ikke altid detaljeret information om de mellemliggende trin, der fører til fejlen. Ved vurdering af pålidelighed af elektronik er det vigtigt at kunne se såvel årsager som effekten af fejl, for at forstå de væsentligste faktorer bag fejlmekanismen. Hovedfokus for dette arbejde er at vurdere elektrokemisk impedans spektroskopi (EIS) som en alternativ og ikke-destruktiv testmetode i forhold til jævnstrømsmetoder. Det primære formål med EIS-tilgangen er at kunne karakterisere dannelsen af et tyndt vandlag på overfladen af et printkort. Da EIS kan skelne mellem forskellige resistive og kapacitive processer og tilstande på printkort under bestemte temperatur- og fugtighedsforhold, kan dannelsen af vandfilm overvåges. Denne vandfilm er forudsætningen for, at elektrokemisk migration kan forekomme, og årsagen til andre fugtrelaterede printkort fejl, ligesom forståelse og kontrol af vandfilmopbygning kan være medvirkende til at kunne forbedre printkort designet for bedre pålidelighed allerede i de tidlige stadier af elektronikudvikling.

Kapitel 1 giver en introduktion til klimatiske pålidelighedstest og omfanget af det arbejde, der udføres inden for dette ph.d.-projekt. I kapitel 2 er det grundlæggende i udvikling af bilelektronik opsummeret, og de relevante fugtighedsrelaterede aspekter er dækket. Derudover beskrives fugtrelaterede fejlmekanismer i printkort sammenhængen, og metoderne til klimapålidelighedstest forklares. Kapitel 3 opsummerer litteraturgennemgangen i lyset af formålet med ph.d.-projektet. Kapitel 4 opsummerer de materialer og metoder, der anvendes som en del af de forskellige aktiviteter i projektet. Forskellige resultater fra forskningsarbejdet er repræsenteret i form af manuskripter, der er beregnet til offentliggørelse i internationale tidsskrifter. Kapitel 5 opsummerer hvert af manuskripterne med de vigtigste mål og resultater, inden manuskripter findes som vedhæftet i de følgende kapitler 6-9. I manuskript 1 spores vandlagets ophobning på en laminatoverflade ved EIS-måling og er relateret til forekomst af elektrokemisk migration ved anvendelse af en jævnstrømsbaseret tilgang. I manuskript 2 anvendes en målemetode for EIS og DC-test til at give en detaljeret allokering af sekventiel vandlagsopbygning og elektrokemisk migration jævnstrøm. Manuskript 3 omhandler lokaliseringen af kondensering på printkort overflader på grund af en temperaturprofil eller tilstedeværelsen af forurenende stoffer. Impedans spektroskopi og Time Domain Reflectometry anvendes til at vurdere indflydelsen af disse parametre. I manuskript 4 forsøges en omfattende evaluering af EIS-teknikken med hensyn til muligheden for at bestemme klimatisk pålidelighed. Dette inkluderer en gennemgang af litteraturinformation samt omfattende evaluering af resultaterne fra manuskripter 1-3 og yderligere evaluering med henblik på muligheden for at bruge EIS som en supplerende

tilgang til jævnstrømstest. Kapitel 10 og kapitel 11 giver en generel diskussion og afslutning af arbejdet og i kapitel 12; forslag til fremtidigt arbejde gives.

Samlet set viser resultaterne fra undersøgelserne vigtigheden af at benytte optimerede testmetoder for at opnå dybere forståelse af klimatisk pålidelighed af elektronik. Det blev demonstreret, at EIS som en alternativ tilgang til den konventionelle jævnstrøm baserede SIR (Surface Insulation Resistance) metode er en effektiv metode til vurdering af fugt stabilitet af printkort. EIS-metoden kan detektere kritiske fugt tilstande inden signalændringer ses ved jævnstrømsmetoder. Ved at sammenligne med den konventionelle SIR målemetode vises forskellen mellem metoderne. En dybere forståelse af printkort designparametre, såsom overfladeegenskaber og forureningspåvirkning, såvel som klimatiske testbetingelser individuelt og kombineret kunne opnås. Det blev vist, at det er muligt at beskrive et årsag-virkningsforhold for fejl og evaluering af resistive og kapacitive systemegenskaber. Kondensationsprocessen og opbygningen af en vandfilm og dermed forudsætningen for fejlmekanismer som elektrokemisk migration kan bestemmes af EIS-tærskelværdier uden faktisk at producere fejlen. I dette omfang tilrådes EIS-teknikken som en standardiseret metode til vurdering af effekten af fugt på printkort.

LIST OF ABBREVIATIONS

ABS	Antilock Brake System
AC	Alternating Current
AH	Absolute Humidity
BGA	Ball Grid Array
CAF	Conductive Anodic Filament
CAH	Contact Angle Hysteresis
CNC	Computer Numerical Control
CPE	Constant Phase Element
DASy	Driver Assistance System
DC	Direct Current
ECM	Electrochemical Migration
ECU	Engine Control Unit
EIS	Electrochemical Impedance Spectroscopy
ENIG	Electroless Nickel/Immersion Gold
ESP	Electronic Stability Program
FR	Flame Retardant
HASL	Hot Air Solder Levelling
IHP	Inner Helmholtz Plane
IPC	Association Connecting Electronics Industries, formerly Institute For Printed Circuits
LC	Leakage Current
LTCC	Low Temperature Cofired Ceramics
MTTD	Mean Time To Dendrite
MTTF	Mean Time To Failure
NTF	No Trouble Found
OHP	Outer Helmholtz Plane
OSP	Organic Solderability Preservative
PCB	Printed Circuit Board

PCBA	Printed Circuit Board Assembly
PI	Polyimide
PTFE	Polytetrafluoroethylene
PWB	Printed Wiring Board
RH	Relative Humidity
RoHS	Restriction of Hazardous Substances Directive
ROSE	Resistivity of Solvent Extract
SAC	Tin-Silver-Copper
SEM	Scanning Electron Microscope
SIR	Surface Insulation Resistance
SMD	Surface-Mounted Device
SMT	Surface Mount Technology
SPR	Surface Plasmon Resonance
TCS	Traction Control System
TDR	Time Domain Reflectometry
THB	Temperature Humidity Bias
THT	Through Hole Technology
TNI	Trouble Not Identified
VOC	Volatile Organic Compound
WOA	Weak Organic Acid

LIST OF PUBLICATIONS

THE FOLLOWING ARTICLES CONSTITUTE A PART OF THIS THESIS

1. **S. Lauser**, T. M. M. Richter, V. Verdingovas and R. Ambat, “Combined EIS and DC Leakage Current measurements to evaluate the process of water film formation and subsequent dendrite growth on electronic assemblies,” under revision in *IEEE Transactions on Device and Materials Reliability*, 2020.

2. **S. Lauser**, T. M. M. Richter, V. Verdingovas and R. Ambat, “Combined approach of EIS with intermittent DC to evaluate the electrochemical migration risk of PCB test boards under condensing conditions,” under revision in *Corrosion Science*, 2020.

3. **S. Lauser**, T. M. M. Richter, V. Verdingovas, R. Ambat, S. Lange, and Y. Grau, “Non-destructive electrical approaches to localize condensation events on PCBs,” draft to be submitted to *Microelectronics Reliability*.

4. **S. Lauser**, T. M. M. Richter, V. Verdingovas and R. Ambat, “On the feasibility of Electrochemical Impedance Spectroscopy to assess climatic reliability of Printed Circuit Board Assemblies,” draft to be submitted to *IEEE Transactions on Device and Materials Reliability*.

CONFERENCE PROCEEDINGS

1. **S. Lauser**, P. Eckold, T. M. M. Richter, V. Verdingovas and R. Ambat, “Implementation of electrochemical impedance spectroscopy (EIS) for assessment of humidity induced failure mechanisms on PCBAs,” *Proceedings of the European Corrosion Congress EUROCORR*, Krakow, Poland, 2018.

2. **S. Lauser**, T. M. M. Richter, V. Verdingovas and R. Ambat, “Electrochemical Impedance Spectroscopy (EIS) for monitoring the water load on PCBAs under cycling condensing conditions to predict electrochemical migration under DC loads,” *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, Las Vegas, USA, 2019.

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1. INTRODUCTION

1.1. BACKGROUND

More than 20 years ago, in the late 1990's, the largest American automobile manufacturer General Motors made a decision that would tragically go down in history of the corporation. They made Takata - an at that time little known Japanese supplier - the new provider of their airbags. Takata undercut the prices of the original supplier, the Swedish-American company Autoliv. In the following years, 16 deaths and more than 180 injuries occurred due to unintended airbag explosions in General Motors cars during driving. They were linked to the use of ammonium nitrate as propellant, which under the exposure to moisture and elevated temperatures, lead to an explosion hazard due corrosive processes [1,2].

Today, even more than then, electronic setups undergo various reliability tests to prevent such failures before they are brought into the field. Numerous regulations and standardized protocols describe the testing procedures, not only for electronics in the transportation sector but also in other domains like industrial technology or consumer goods. However, the automotive electronics field is especially affected, because products like airbags or braking systems have life-preserving functions and are produced in high quantities. Testing is also particularly relevant, as exposure to reliability-critical parameters like temperature, humidity or vibration can be manifold during the lifetime of a product. Especially the risk of humidity induced failures is as relevant as ever. Novel trends towards miniaturization, the need for new materials in electronics and their wide-spread use in different vehicles all over the world result in the exposure to various climatic conditions. These can cause different humidity related reliability issues due to corrosion. In many cases, the precondition for these corrosive failures is the formation of a thin water film on the electronics main component, the Printed Circuit Board Assembly (PCBA). The condensation process and water film buildup is affected by a variation of transient climate parameters, such as local temperature and humidity. Likewise, inherent factors of the PCBA itself determine the water layer formation, its properties, and the potential corrosion. These include aspects resulting from miniaturization efforts and the use of different materials. Distances between biased points on the PCB become narrower due to miniaturization efforts, which makes it easy for a transient water film to connect between biased points. Material and design related factors, like the use of solder mask or coatings affect the water film buildup under humid conditions. The use of the no-clean flux chemistry for soldering entails in the presence of water-absorbing hygroscopic residues after the manufacturing process. These contaminants change the chemistry of the PCBA surface in a way that water adsorption is enhanced and additionally their impact on the electrical properties of a thin water film can reinforce corrosive processes.

The electrochemical conditions of the micro-cell formed on the PCBA surface between neighboring points of different potential bias, such as component legs or soldered connections acting as electrodes, essentially determine the corrosion criticality. The electrochemical sequences of the corrosion process are affected by various factors: (i) faradaic reactions at the electrodes connected by the water film, (ii) ion transport limitation due to the low thickness of the water film, (iii) stability of dissolved metal complexes due to local pH changes and (iv) conductivity of the film itself, depending on dissolved ions. Depending on the mentioned parameters and local humidity and temperature, the water layer thickness formed under humid conditions can vary from the fraction of nanometer scale to hundredths of nanometer. With the water acting as electrolyte medium, various electrochemical processes that interfere with the functionality of the PCBA are likely to occur. Involved failure mechanisms can be simple leak current failures due to lowered surface resistance once a water film has built up. If condensing conditions are kept up long enough, water adsorption can proceed until an established film forms, bridging electrodes (Figure 1.1a)–c)). With a pronounced established water layer, it can act as an electrolyte and enables electrochemical migration (ECM) between electrodes if they are oppositely biased (Figure 1.1d)). ECM describes the process metal oxidation at the anode, metal ion transport through the solution within the electrical field and the deposition of metal at the cathode. If it is given enough time, this can result in the formation of short circuits on the PCB, due to a dendrite formation between the potentials (Figure 1.1e)). Thus, the failure sequence is primarily affected by an interplay of a critical level of water film buildup and the PCBA parameters such as electrical field (determined by pitch distances and potential bias), surface morphology and cleanliness. Therefore, understanding and controlling the water film buildup and a knowledge on the sequential changes in the electrochemical aspects that lead to ECM is what essentially supports the prevention of humidity related failures in electronics [3–6].

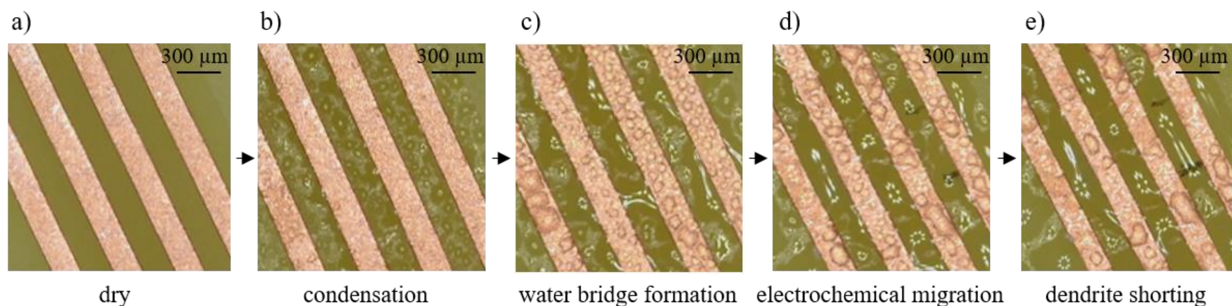


Figure 1.1: Sequential steps of condensation, water bridge formation, electrochemical migration and dendrite shorting between interdigital copper electrodes on an FR-4 PCB surface.

In material development and process qualification, test methods that are used to assess such failures are commonly based on the application of a DC (Direct Current) voltage and measurement of leakage currents on specially designed test structures in different climatic scenarios. This approach is also referred to as

Surface Insulation Resistance (SIR) test, as a drop in SIR can be traced back to a corrosion-critical state. However, the DC methods seldom provide information on the water film buildup and its characteristic properties. This is because under DC technique, a high potential level is applied to the system, causing polarization of the electrodes. Hence, the corrosion process itself is provoked and short-circuiting due to dendrite formation is detected. However, the polarization masks the information related to the required water film. Establishment of a root-cause relationship of ECM, encompassing all influencing parameters such as the kinetics of the water film buildup is therefore not possible in the DC mode [7,8]. To overcome the drawbacks of the DC method, techniques, which are based on the application of an alternating voltage, can be another approach. Electrochemical Impedance Spectroscopy (EIS) in particular is an AC (Alternating Current) method that applies an alternating signal of a low mV amplitude over an arbitrary wide frequency range. The system's complex impedance |Z|, governed by resistive, capacitive and inductive properties, determines the output signal. Their changes during the condensation process on a board, allow a detailed characterization of the water film buildup and the electrical nature of the water layer [8]. Therefore, it could be a suitable method for studying the humidity related effects on electronics, as it also comes with the benefit of being non-destructive to the specimen due to the low AC signal. For this reason, the main scope of this PhD project is to use EIS as an alternative technique to DC measurements. EIS is applied to understand the humidity interaction with PCBAs, while also investigated for its feasibility and capability to predict humidity induced failures. The aim of this work is to contribute to the implementation of EIS in the reliability testing of electronics for future applications.

1.2. SCOPE OF THE THESIS

This study focusses on the comprehensive understanding of condensation processes forming a thin water film on a PCBA surface and the accompanying or subsequent processes leading to electronics failure. The main objective is the measurement of the electrical properties of the water film building up and the correlation of the information with ECM occurrence in order to know the critical water film level (Figure 1.2). For this purpose, the influence of different aspects like PCBA design parameters, materials and cleanliness are investigated. With a measurement setup that allows exposing samples to different climatic conditions in terms of temperature and relative humidity, the stepwise condensation and water film buildup is characterized for its electrical properties by electrochemical means. In particular, Electrochemical Impedance Spectroscopy (EIS) as AC technique is applied to investigate the resistive and dielectric behavior of the system upon water layer formation. Based upon an understanding of the kinetics related to water film buildup and the respective resistive and capacitive changes in the system, a comparison of the EIS method and DC measurements for humidity robustness valuation have been evaluated. Within this framework, the eligibility of EIS as an alternative for the DC method is assessed.

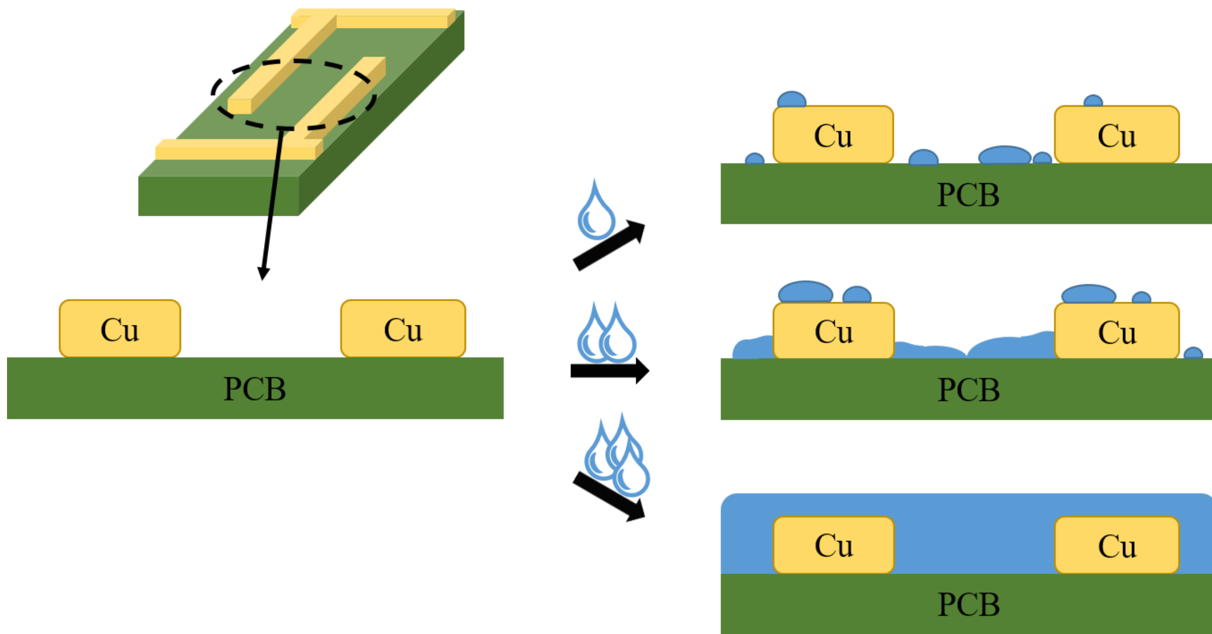


Figure 1.2: Schematic representation of different levels of water film formation on a PCB surface between adjacent copper tracks.

The detailed research focus of this PhD thesis includes:

- Different PCBA parameters, among them substrate materials (chemistry, morphology), pitch distances, contamination and solder joint-covering components are tested in terms of their impact on water film formation. Varying temperature and humidity states are provoked throughout the testing, in order to achieve different non-condensing and condensing conditions on the PCBs. The water layer buildup and its electrical properties are investigated using EIS and compared with results from parallel or intermittent DC measurements. For this purpose, PCBA samples are designed, starting from the simple setups, going to specimen with higher complexity with regard to combining the mentioned parameters. This way, a comprehensive understanding of the variables added to the system and the effect on water film formation is targeted.

- By means of AC impedance spectroscopy and Time Domain Reflectometry, a localization of enhanced condensation in PCBA areas of different surface temperature distribution and different contamination levels is pursued. Their impact factor on the severity of condensation can be evidenced. By means of impedance measurement, ECM-safe distances to heat sources like powered components are determined. TDR measurements localize enhanced condensation at spots of flux contamination along conductor traces by a local impedance decrease.

- In addition to electrochemical measurements, samples are analyzed by means of in-situ optical microscopy in order to comprehend the level of condensation and to track the closing status of a water bridge, corresponding to the electrochemical data.
- Different levels of water load are measured gravimetrically to obtain an average water layer thickness and associate the corresponding EIS and DC data.
- As of optical measurements after testing, samples are analyzed partially by cross-section or surface view. They are reviewed in terms of corrosion products to gain supplemental knowledge on the occurring electrochemical processes under water film.
- A correlation between the results of the EIS measurements and the sample parameters that lead to a specific failure mode upon DC testing is to be established from the conducted tests and analyses. In doing so, the aim is to understand which transition point in the water film formation leads to transient failures on a specific PCBA.

Seeking a possibility to replace the time consuming, statistically elaborate and resource-consuming SIR measurements of PCBs as a criterion for a specific humidity robustness, a correlation between EIS and DC measurements needs to be evaluated. The idea is to use EIS for understanding the cause-effect relationship between water film buildup and electrochemical failure. This way, the method can be established to characterize conductive processes on the PCBA without causing irreversible reactions as during DC measurements. EIS allows the screening of a system under different humidity conditions in much shorter time, with fewer samples and higher confidence level. This way, the translation of EIS measurement data on water film formation and respectively occurring electrochemical processes can also be used to filter out critical PCBA setups in early development stages.

1.3. STRUCTURE OF THE THESIS

The thesis is divided into twelve chapters, as presented in Figure 1.3. Chapters 1-3 introduce the topic, give an outline on the related literature and summarize the aim of the project with regard to the state of the art. The materials and experimental methods that were utilized for the work are presented in chapter 4. In chapter 5, the papers that include the conducted studies as part of the thesis are summarized with their objectives and findings. The papers are then appended in chapters 6 – 9 in the form of manuscripts submitted, or intended for journal publications. Chapter 6 provides an insight into the capabilities of EIS to detect water film formation and relates the findings with results from DC testing in terms of dendritic growth. In chapter 7, a measurement approach of alternating EIS and DC testing to provide a detailed allocation of the water bridge status on a board and the onset of ECM is presented. Chapter 8 shows the

possibilities to localize condensation events, governed by surface temperature distribution or surface impurities by means of non-destructive techniques. Chapter 9 presents a general overview on the feasibility of EIS to assess climatic reliability of PCBAs. The advantages and disadvantages of the EIS method in relation to conventional DC SIR testing are reviewed. An overall discussion and conclusion is depicted in chapters 10 and 11. Chapter 12 provides an outlook with recommendations for future work based on the outcomes of the thesis.

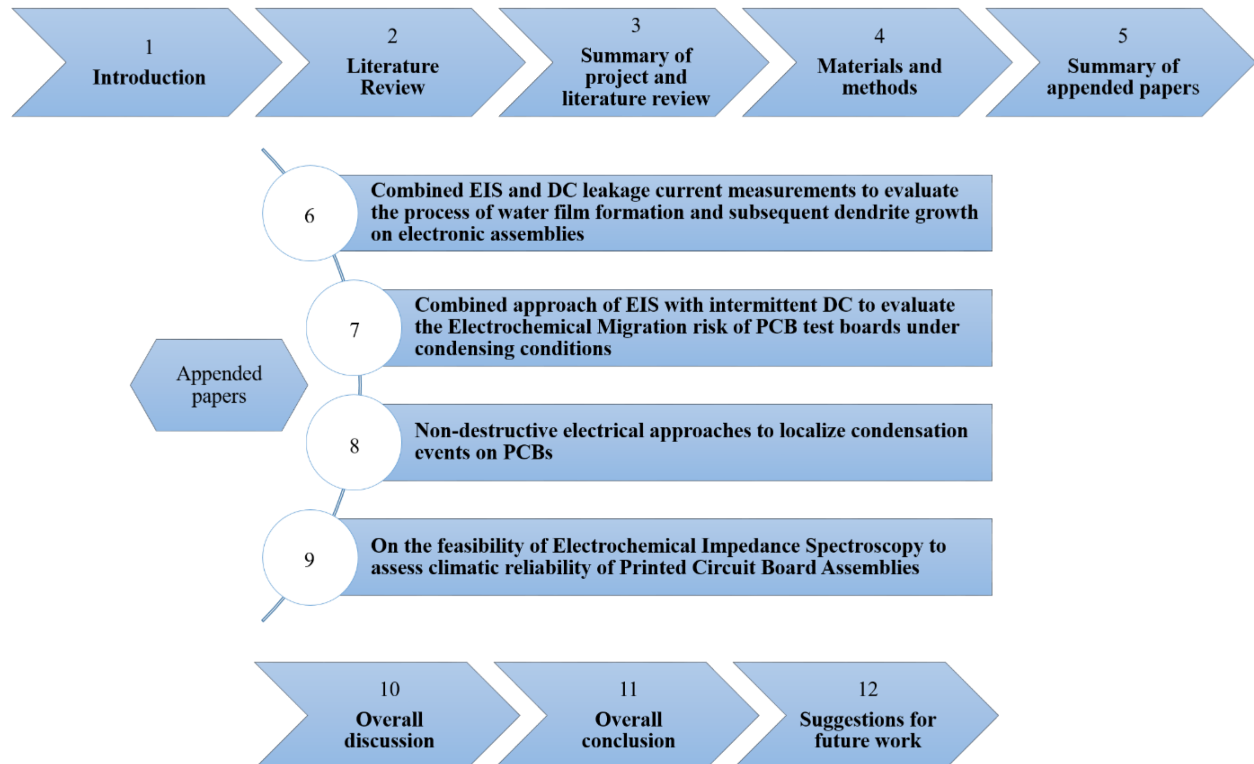


Figure 1.3: Schematic overview of structure of the thesis.

2. LITERATURE REVIEW

2.1. AUTOMOTIVE ELECTRONICS

In the development of transportation vehicles, various electronic devices are in use. Considering the automotive sector, the use of electronics for different functionality can be divided into the parts related to drivetrain, communication, safety, and comfort. An exemplary listing of common electronics for each sector is shown in Table 2-1 [9].

Table 2-1: Exemplary automotive electronics in a motor vehicle in the sections drivetrain, communication, safety and comfort [9].

Drivetrain	**Communication**	**Safety**	**Comfort**
Electronic transmission control	Navigation	Electronic Stability Program (ESP)	Adaptive Cruise Control
On-board-diagnosis	Electronic voice output	Antilock Brake System (ABS)	Chassis Control System
Gasoline engine: motronic	Audio equipment	Traction Control System (TCS)	Heating and air-conditioning
Diesel engine: electronic	Car phone	Wash-wipe control	Central locking

Over the last fifty years, the use of such electronics has drastically increased. Today's standard vehicles have surpassed the capabilities of the Apollo Lunar module that landed first humans on the moon in 1969 [9]. Especially within the last decade, emerging trends primarily related to the electrification of the vehicles have led to great changes in the sector. These include not only improvements in the conventional combustion engine powertrain, but also new approaches like fully electric drives or hybrid systems. By 2020, most of the conventional automotive manufacturers have an electric model in their portfolio [10]. Huge progress has also been made in the context of autonomous driving. First successes in this field can be dated back to the 1990s, when a coast-coast drive across the United States of America was achieved by a vehicle largely automated [11]. The fact that an autonomous vehicle needs to unite environmental perception and driving behavior puts high demands on related electronics. Therefore, different monitoring approaches such as laser (LIDAR) and radar (RADAR) systems come to use. Computational requirements to process the obtained data lead to highly complex electronics [12]. Even though fully autonomous driving is still an issue of law in many countries and circumstances, US-states like Florida have legally facilitated the establishment of self-driving cars [13]. In some countries, it is already possible to have semi-autonomous components in a vehicle. It is to be anticipated that this progression from driving semi-autonomously to full autonomous driving will be completed within the next decade. Respective advancements in electronics to deliver reliable setups are driving the industries in the automotive sectors.

All of the factors mentioned, along with continuous miniaturization of electronics as well as evolution of new materials lead to an increased number and complexity of electronics in an automobile. Exemplarily, the automotive electronic products of a 2019 generation are schematically represented in a glass car in Figure 2.1.

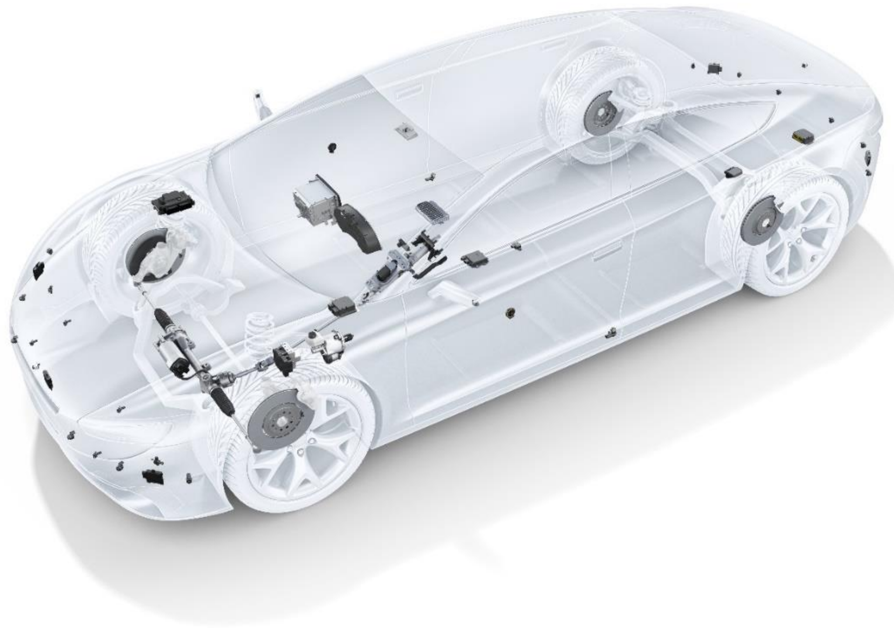


Figure 2.1: Glass car representation of automotive electronics product generation in 2019 [14].

Novel components among them are multi-purpose cameras (MPCs), an electromechanical brake booster, ultrasound and radar sensors, and the driver assistance system domain controller (DASy), collecting the sensor data for assisted and automated driving.

The main component of most electronic setups that come to use in a transportation vehicle are Printed Circuit Board Assemblies (PCBAs), packaged in a housing. An example of this concept is shown for an Airbag Engine Control Unit (ECU) in Figure 2.2. The PCB shows a variety of assembled components. A plug is attached for outward connection through the housing.

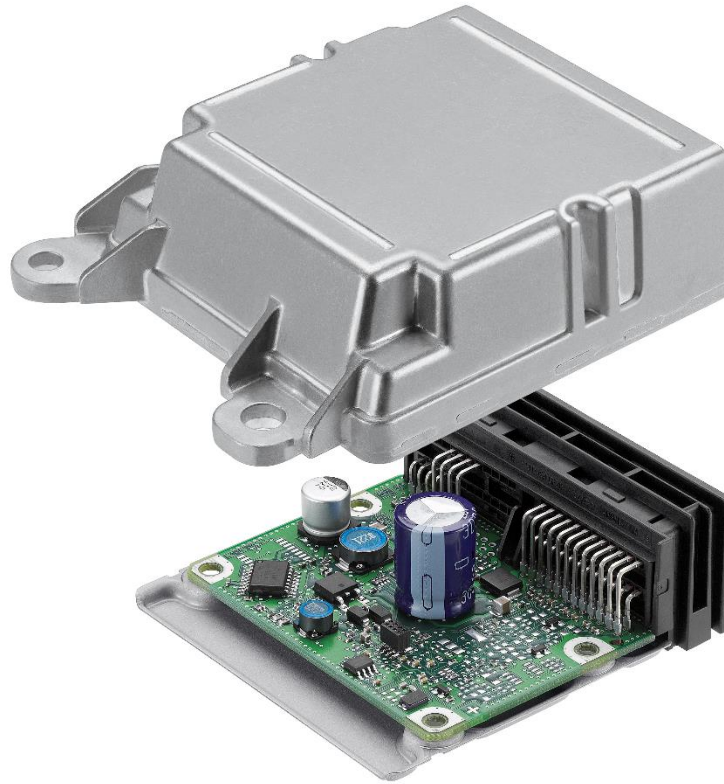


Figure 2.2: Magnified view of an Airbag Engine Control Unit. Printed Circuit Board with assembled components, attached plug for connection outward of the housing [14].

In the development of a new setup, the manufacturing process of the PCBA and all of the utilized materials are carefully investigated for their processability and functionality. The employed manufacturing technology and materials are presented in the following two sections.

2.1.1 PCBA Manufacturing

A printed circuit board (PCB) is a mechanical and electrical support for interconnecting electronic components by conductive tracks. The tracks are etched from metal sheets laminated onto a non-conductive laminate, functioning as substrate. Typical PCB thicknesses are in the rage of 1.5 mm. A common material for the tracks is copper [15]. If a board with mounted components is considered, this is referred to as printed circuit board assembly (PCBA). A PCB can be single-layered, double-layered (top layer is aligned with bottom layer, holes are drilled through board and copper is deposited subsequently to connect top and bottom layer) or multi-layered (stacked individual copper patterned laminates). A typical PCB generally consist of four different materials: base material, copper, solder mask and surface finish (Figure 2.3).

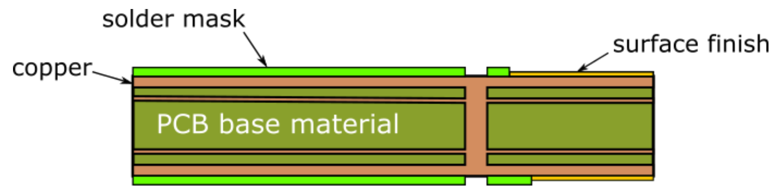


Figure 2.3: Exemplary PCB buildup comprised of base material, copper conducting layers with surface finish at exposed areas or covered with solder mask.

The PCB base material is an electrically insulating material (typically fiberglass, reinforced with resin), which serves as substrate for the copper conducting tracks. The polymer solder mask restrains solder spreading and can serve the enhancement of surface insulation resistance. An organic or metal surface finish is applied onto the surface of copper layers to prevent them from oxidizing. Upon solder mask application, the individual PCBs can be cut out of the panel with a computer numerical control (CNC) machine.

In assembly of a PCBA, there are different possibilities of attaching functional components. Generally, in solder board assembly, two automated ways of mounting are distinguished: Surface Mount Technology (SMT) and Through Hole Technology (THT). In the case of surface mounting, the surface mount devices (SMDs) are fixed by soldering their metallic terminations to pads on the board. In THT, the components have leads that are fixed through holes in the board [16]. Compared to THT, SMT comes with the advantages of higher packaging densities, a better electrical performance, and the possibility to greatly automate assembly, resulting in a faster manufacturing process.

In SMT, the paste required for soldering is transferred to the designated pad areas of the PCB, using a metal stencil with pad-size openings. Usually the openings in the stencil are fabricated by laser-cutting [17]. The volume of an opening determines how much solder paste is transferred to a pad. During the paste printing process, the stencil is placed on the PCB and then the solder paste is pushed over the stencil with a squeegee to fill the openings (Figure 2.4). Afterwards, the stencil is removed and the quality of the print can be inspected (2D or 3D).

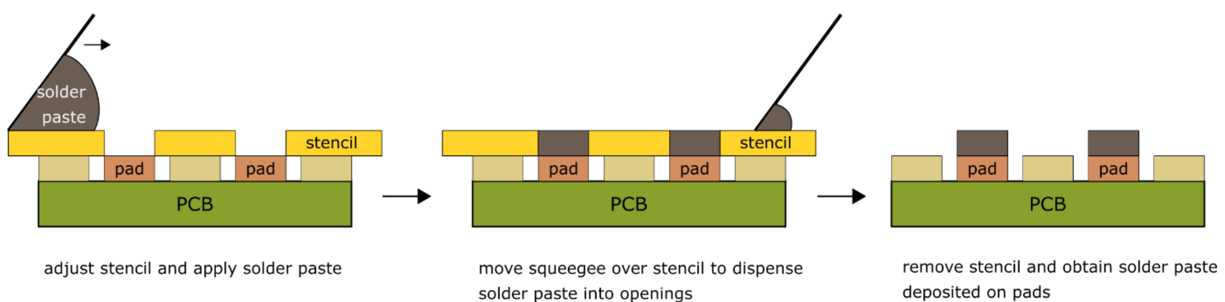


Figure 2.4: Procedure of solder paste printing process on the PCB surface for reflow soldering.

The shape of the paste, fitting to the opening in the stencil and a good coverage of the pad with solder paste, determine a good printing quality. The volume of the paste should be adjusted in a way that there is no paste remaining on top of the stencil nor within the stencil openings after printing. Following the printing process, the electronic components are placed on top of the solder paste on the pads. During the soldering process, the solder paste is melted to create an electrical and mechanical connection between component and pad. This process takes place in special furnaces, through which the PCBs are transported with a chain-transport system. The oven is typically divided into different zones to allow the exposure of a certain temperature profile. Different component classes might require different temperature profiles in terms of peak shape and cooling rates. A reflow can be conducted for both sides of a PCB, the PCBs are then turned over after the first side is soldered and the component assembly steps are carried out again on the second side. During the reflow step, a specific temperature profile is applied to the PCB. An example is displayed in Figure 2.5 for SnAgCu (SAC) solder paste and eutectic SnPb [18].

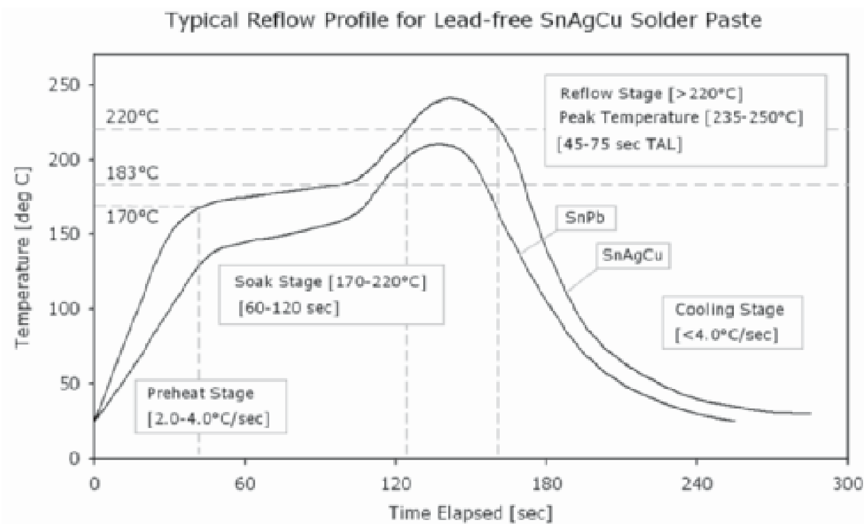


Figure 2.5: Typical temperature profile for reflow soldering of leadfree SnAgCu solder paste and eutectic SnPb [18].

The heat transfer can be based on convection only (e.g. circulation of hot gas, usually mainly Nitrogen to avoid oxidation) or based on radiation or conduction (for example by IR-radiation or vapor phase soldering). During temperature ramp-up, the volatile parts of the solder paste evaporate. The liquefied metal wets the surfaces of component and pad. When the temperature is reduced again, the metal solidifies to form a solder joint between substrate and SMT component.

In the THT soldering process, components with pin-like lead wire can be mounted through board holes. If a PCB also contains through hole components, they are assembled after the SMD components and are soldered selectively. THT components are primarily larger components like coils or electrolytic capacitors.

The common process used for THT components is wave soldering. The components are usually placed onto an adhesive layer to stick to the PCB during the process [19]. Wave soldering can be used not only for selectively mounting some components but also for whole PCBAs, although the process characteristics for both cases are similar. The first step of wave soldering is fluxing. Flux can be deposited by brushing or spraying in the designated areas depending on whether the soldering is for the whole PCBA or selective. During a preheating step, the flux is activated, the volatile components evaporate and the surface oxides are removed. Following the pre-heating, the bottom part of the PCBA is exposed to a solder wave at peak temperature in order to achieve the soldering. A turbulent flow on top of the solder nozzle ensures a continuous heat transfer throughout the nozzle, leading to a better solder efficiency. A possibility for the control of THT solder joints after the solder process is a manual inspection by eye or microscope. This is feasible for failures like missing pins, solder bridges or washed off components [16]. In the manufacturing of an electronic unit as displayed in Figure 2.2 often all of the mentioned process come to use. Small SMD-components are assembled by reflow soldering, while larger components like electrolyte capacitors are mounted with wave soldering techniques. The mounting of connectors is normally accomplished by press fit joints.

2.1.2 PCBA Materials

<u>PCB laminate</u>

The base laminate of a PCBA is an insulating dielectric substrate. Most commonly, epoxy resin with interwoven glass fibers is used (Figure 2.6). There are different possibilities of adjusting mechanical and electrical properties, depending on the use case and cost requirements. Standard FR-4 laminate has a surface resistance in the range of 10^4 MOhm and dielectric constants ε_r typically between 4.6 – 4.9. A higher quality version like FR-408 has a surface resistance value of at least 10^6 MOhm and a dielectric constant ε_r of 3.8. For electrical connection, Cu is the most used material to laminate sheets to the base material. In terms of design and layout, most manufacturers have distinct guidelines. Typical best capabilities in the area of minimum track and gap width of Cu are around 100 µm [16].

Figure 2.6: Exemplary cross section of an FR-4 laminate consisting of epoxy resin with interwoven glass fibers.

A so-called "surface finish" standardly covers the PCB laminate. It has the primary goal of protecting exposed Cu from oxidation or degradation and enabling its solderability during PCBA manufacturing. There are numerous kinds of finishes. Some common ones are Immersion Silver (ImAg), Immersion Tin, Electroless Nickel/Immersion Gold (ENIG), Hot Air Solder Leveling (HASL) and Organic Solderability Preservative (OSP). ImAg and Immersion Tin provide planar surfaces, are applicable for fine pitch distances and comparably inexpensive. ENIG comes with the same advantages, and additionally enables good thickness control; however, it is more expensive than the other finishes. The HASL finish shows good solderability and comes with the advantage of a long shelf life. On the downside, it often shows an uneven coating distribution and is therefore not suitable for fine pitch distances. The OSP shows excellent applicability for fine pitch distances but is in turn limited in shelf life.

Solder Paste

Solder paste is used to interconnect SMT with the electrical circuitry on a PCB. In case of a reflow soldering process, it is composed of metal powder (85 – 90 Weight-%, 40 – 50 Vol-%) and flux. The metal alloy forms the electrical and mechanical bond between solder pad and component. A typical composition of the weight-% contents of a paste is displayed in Figure 2.7.

Figure 2.7: Typical weight-% composition of a SMT solder paste [20].

Chemical composition of the metal powder varies, depending on the intended use and required reliability. It can consist of lead, tin, silver, copper or nickel based alloys or others. Small amounts of other metals like bismuth can be added to tailor the paste's characteristics, for example affect the melting temperature [20]. Most conventional solder systems have been based on Sn-Pb alloys. However due to restrictions in Pb use by the European Union, nowadays SnAgCu (SAC) alloys are used more intensively [21]. It is a near eutectic system with a melting point in the range of 217 °C for an Ag-content of $3 - 4$ % and a Cu-content of $0.5 - 1$ %, laying approx. 34 K higher than that of Sn-Pb. If there is an additive of Bi and Ni in the alloy, the system is referred to as Innolot. It comes with the advantage of a slightly reduced processing temperature compared to pure SAC [20]. For SAC-based solder pastes, particularly in comparison with Sn-Pb pastes, the thermal-fatigue performance has shown to be improved in accelerated tests [22]. In the soak stage of a reflow process (Figure 2.5), the solvents in the paste are supposed to evaporate; flux is activated, reduces surface oxides and evaporates. Careful adjustment of the profile is crucial to assure the persisting

de-oxidation characteristics of the flux. The flux in the solder paste accomplishes the tasks of surface oxide removal, prevention of re-oxidation at the soldering temperatures, assisting in heat transfer at the forming joint and improving the wettability of the joint surface. The active chemicals in the flux are commonly organic acids, halides or amides that are activated during heating. They enable a direct contact between the metal surface and the solder by cracking and removing the oxide layers, generating e.g. salts and water. The resin matrix is used to encapsulate unreacted activators and the ions that result from chemical reactions during the solder process and by this improve the joint's reliability in terms of chemical migration processes. Solvents come to use to regulate the viscosity of the paste. Typical materials are polyethylene glycols. Thixotropic agents regulate the printing behavior, as they change their viscosity with the applied shear force. Other additives can be added to control various properties of the solder paste. They include surfactants, corrosion inhibitors or stabilizers. In wave soldering, generally a similar kind of SMT flux composition is used, however in the form of a liquid. Albeit, it is applied typically by spraying, prior to the preheat phase and the immersion of the board in the solder wave. However, the activity of the flux is usually higher, having a greater amount of additional liquid activators [23]. Nowadays, most solder pastes are so called no-clean pastes, claiming that no critical residues are left on the board after soldering. Still, a complete removal of residues or the encapsulation of all critical chemical components is not easily given [24]. Accordingly, in the context of PCBA reliability, fluxes are associated with potential risks especially in humid environment or transient dewing conditions. The problems that arise thereby are described in detail in Chapter 2.3.

Solder Mask

The solder mask is a polymeric layer usually made of epoxy that is applied to the PCB surface as protective coating. One of its tasks is to prevent formation of bridges between neighboring solder pads by offering a non-wetting surface for molten solder material [19]. It is also supposed to protect laminate and contacts from contamination or material degradation. Additionally it serves insulating purposes between components and conducting tracks. Most solder mask materials are two-component systems, comprised of a multifunctional binder and an epoxy resin. They are usually UV-cured, meaning photoinitiators react with the resin.

2.2. HUMIDITY

2.2.1 Characteristics of moisture and interaction with surfaces

Humidity is described as the water vapor content present in the air. A distinction is drawn between absolute humidity, specific humidity, and relative humidity. Absolute humidity (*aH*) is also referred to as vapor concentration or vapor density. It describes the ratio of water vapor mass m_{H_2O} to a distinct volume of

air V_{air} (Equation 2.1). Relative humidity (*rH*) is the dimensionless ratio of the water vapor partial pressure p_p to the saturation vapor pressure p_s. It is dependent on the temperature and the air pressure, meaning at low temperatures, less water vapor is needed to reach a distinct *rH* than at high temperature. *rH* is often expressed as a percentage (Equation 2.2) [25,26].

$$aH = \frac{m_{H_2O}}{V_{air}} \qquad \text{Equation 2.1}$$

$$rH = 100 \cdot \frac{p_p}{p_s} \qquad \text{Equation 2.2}$$

The ideal gas law, an equation of state, describes air as a gas, stating that at a given temperature *T*, the product of pressure *p* and volume of the gas *V* is constant. Temperature and volume of the gas have a proportional correlation, such as temperature and pressure. At a distinct pressure and temperature, the volume is proportional to the amount of substance of the gas, *n*. These relationships result in the ideal gas equation, with *R* being the specific gas constant (Equation 2.3) [27].

$$pV = nRT \qquad \text{Equation 2.3}$$

To evaluate within a gas system of water vapor in air, a so-called "Mollier diagram" can be used (Figure 2.8).

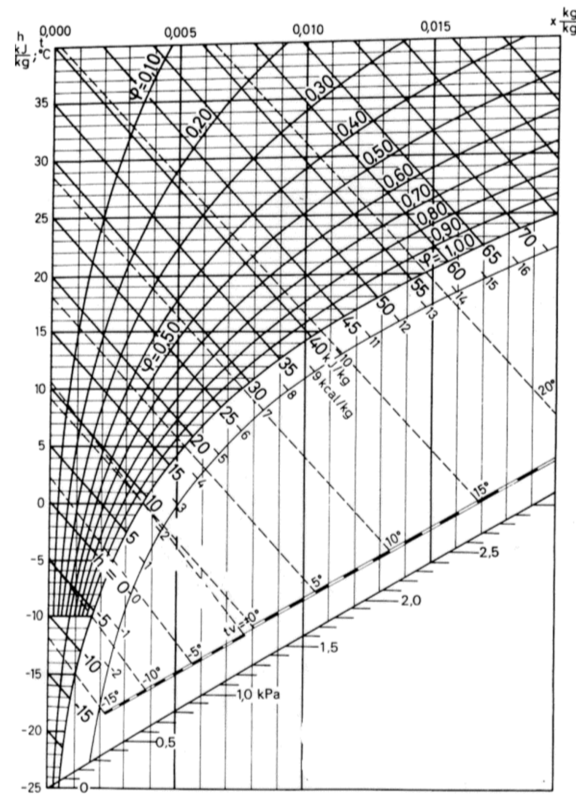


Figure 2.8: Mollier diagram showing the possible states of water vapor in air [28].

All states of humidity can be visualized. The left scale describes the temperature in °C. The upper scale is the absolute humidity in kg/kg. The diagonal lines describe the specific enthalpy. The bent curves visualize the relative humidity in nonpercentage values, meaning it goes from 0 to 1 as in 0 % humidity to 100 % relative humidity when the air is fully saturated. Going beyond this line (φ = 1,00), the air cannot take up any further humidity and condensate formation starts.

The water molecule itself is only approx. 29 Å in size, facilitating penetration interactions with various materials. Additionally, it can serve as both a hydrogen bond donor and acceptor, enabling the formation of hydrogen bond networks. Therefore, when interacting with solids, there are five mechanisms that can be distinguished (Figure 2.9).

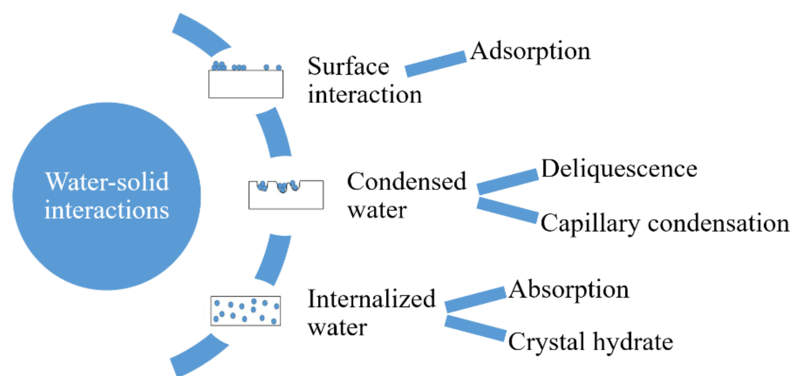


Figure 2.9: Classifications of water-solid interactions, categorization is based on [29].

Considering plain surface interaction, water molecules can be adsorbed. Molecules from a gas phase stick to the solid surface or ions from an electrolytic solution can be attracted to an electrode [30]. The generic term of “condensed water” unites deliquescence and capillary condensation phenomena. Deliquescence describes a first order phase transition from solid medium to solution that occurs at a characteristic *rH*, depending once again on the solid properties and the temperature [29,31]. Capillary condensation describes enhanced condensation into capillaries, as the water is subjected to a suction pressure. Multilayers are stacked above monolayer, hence the molecules are less firmly bound [32,33]. In the context of internalized water, absorption and crystal hydrate are distinguishable, both describing a significant uptake of water into the solid structures [34]. The relation between relative humidity and moisture content can also be represented in the form of moisture sorption isotherms. These can be classified for different materials according to the schematics in Figure 2.10 with the x-axis representing relative humidity and the y-axis the moisture content. Type I describes limited sorption of a few monolayers of adsorbate, for example microporous materials like Zeolites. Type II represents the transition from monolayer to multilayer sorption for non-porous or microporous absorbents like Al_2O_3. Type III describes weak interactions of adsorbent

and adsorbate and deliquescence phenomena. Type IV displays the moisture sorption for porous surfaces, allowing coverage of mesopore-walls and resulting in capillary condensation or pore filling. Type V represents small adsorbate-adsorbent interactions and capillary condensation on porous surfaces. A layer-by-layer adsorption on a uniform substrate is given by the stepped isotherm of Type VI.

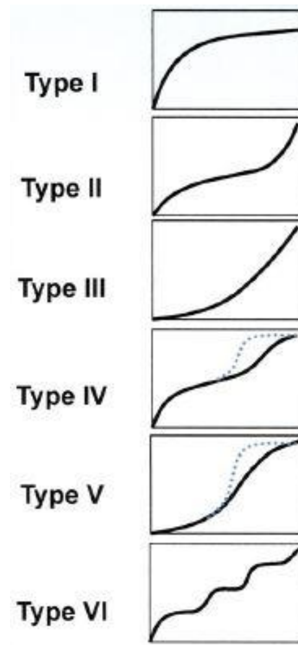


Figure 2.10: Moisture sorption isotherms giving the qualitative relationship between total moisture content (y-axis) and relative humidity (x-axis), classified into Types I-VI [33].

In the context of the humidity effects on electronics causing PCBA surface leak current or failures mechanisms such as ECM, substantial water layer thickness, exceeding the usually absorbed molecular layers, is important. Such conditions can be described as similar to water film formation under high humidity conditions together with material features of the PCBA assisting thicker water film formation or hygroscopic compounds on the PCBA that absorb water. Likewise, differential temperature on the PCBA can result in dew formation. Therefore, the film thickness regimes can be considered similar to near condensation up to full condensation conditions.

2.2.2 Condensation and water film formation

Condensation is a process of phase transition, in which dew is formed. Water vapor from the air is transformed into liquid when it gets in contact with a surface. Generally, the requirement for this to take place is that the temperature of the surface is equal or lower than the dew point temperature [35]. The process of condensation starts with heterogeneous nucleation on a surface. This occurs if water vapor is conditioned to a pressure p_r that is greater than its saturation pressure p_s. The condensation into liquid state

occurs to reach minimal energy. The change in energy for a volume V (= $\frac{4\pi R^3}{3}$, R being the droplet radius) to transform into liquid is $V\Delta e$, with Δe being the change in volume free energy. For this, the energy to establish the liquid-vapor interface is required first. The overall energy balance W_{nuc} is according to Equation 2.4. The first term describes the energy of transformation of the volume into liquid and the second term the formation of the interface with γ being the interfacial tension.

$$W_{nuc} = \frac{-4\pi R^3}{3}\Delta e + 4\pi R2\gamma \qquad \text{Equation 2.4}$$

The energy cost for nucleation exhibits a maximum for a critical radius R^*, according to Equation 2.5. Hence the condensed droplet is only stable for $R > R^*$.

$$R^* = \frac{2\gamma}{\Delta e} \qquad \text{Equation 2.5}$$

An isolated water droplet on a surface grows while forming a depletion region in the surrounding water vapor atmosphere. Considering the case of a single droplet subjected to an atmosphere of constant gas velocity U parallel to the surface, there are different processes that can occur during droplet growth (Figure 2.11). Number 1 indicates direct accommodation of water molecules from the air at the drop surface. Release of latent heat into the substrate leads to formation of a temperature gradient with the maximum gradient being at the phase contact line TL. If the latent heat of condensation cannot be released into the substrate easily, this can slow down or even prevent the growth. Number 2 describes the process of nucleation and evaporation of small droplets with a radius in the range of the critical radius. This leads to a surface diffusion towards the regarded larger drop. Number 3 represents nucleation, growth and merging of small-scale droplets. Eventually, this leads to a feeding of the droplet at its perimeter [36,37].

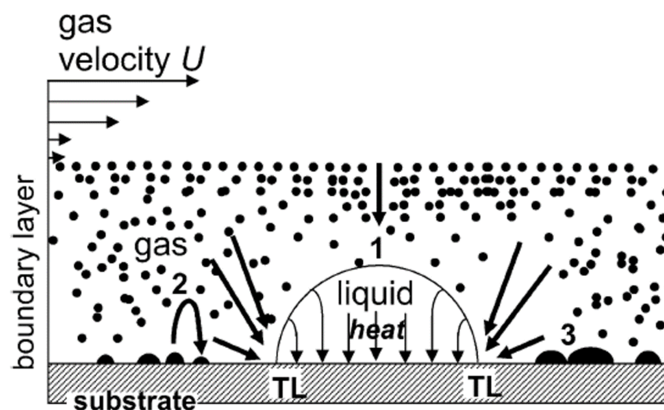


Figure 2.11: Growth of an isolated single droplet, with direct accommodation of water to the drop (1), growth by diffusion of adsorbed water (2) and growth and merging of small-scale droplets that eventually feed the drop (3) [37].

Experiments and simulation of dropwise condensation on polymer and glass substrates also showed that smaller droplets (< 50 µm in diameter) grow by diffusion of adsorbed water to the drop perimeter (Number 2 in Figure 2.11). Droplets that are larger in diameter primarily grow by direct deposition from the water vapor in the air (Number 1 in Figure 2.11) [38].

Considering the droplets in a pattern, neighboring droplets can fuse once their perimeters touch (Figure 2.12). This signifies that periods of continuous droplet growth are interrupted by coalescence events, resulting in a sudden jump. Considering an area of condensing droplets, the condensation rates do not match with those of individual droplet growth or with film-like growth. Instead, each droplet in the pattern has its own growth characteristic, depending on the distinct size and possibility of interacting with neighboring droplets [39]. The merging of droplets results in a so-called "self-similar" regime that relates typically to a droplet surface coverage of 30 %. It describes the state of a constant coverage, which is based on the balancing of two different effects: (i) the proceeding condensation leads to an increase in the droplet radii, increasing also the surface coverage. (ii) The increase in droplet radii results in a higher coalescence probability, thus freeing covered surface, as merged droplets grow in height. The freed space on the surface can provide room for another generation of droplets that grow with an individual rate and increase overall surface coverage [37].

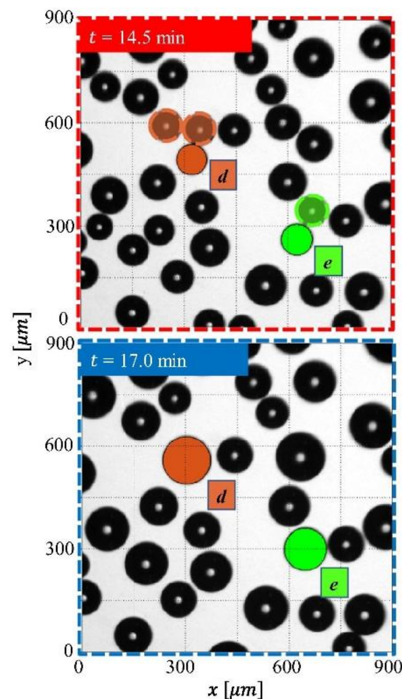


Figure 2.12: Snapshot images of droplets condensing on a silanized silicone substrate with a temperature of 10 °C, a chamber relative humidity of 70 %rH and a temperature of 20.5 °C. Images are shown for droplets d and e before (14.5 min) and after (17 min) their coalescence with neighboring droplets [39].

The described circumstances show that for a comprehension of the condensation process until film formation in detail, the growth of an isolated droplet as displayed in Figure 2.11 does not replicate the actual state. It needs to be considered that neighboring vapor distribution profiles affect the rate of condensation. Going one step further, the condensation process can be regarded in a film-like growth approach. It describes the merging of individual water vapor concentration spheres into a profile parallel to the surface. The pattern is considered as a homogeneous film with a uniform thickness. The process of condensation until water film formation on a surface is fundamentally affected by the surface characteristics. The initial step of droplet nucleation was shown to be influenced by the contact angle of a substrate. It is noted that the lower the contact angle, the more nucleation sites are present on the surface. The merging process of the droplets likewise depends on the surface heterogeneity. Vapor concentration profiles are not uniform across a non-planar surface. Droplets at discontinuities are sitting closer to the water vapor source than droplets in inner edges. However, depending on the shape of the discontinuity, droplet growth can also be enhanced by geometrical modifications of the substrate [37,40].

When considering the condensation process until the buildup of a continuous water bridge across a certain distance or area on a surface, various impact factors on this need to be taken into account. The impact of surface morphology especially for the merging process is depicted in Figure 2.13. The left part represents the process of water film formation across an electrode gap for a rough surface, the right part for a smooth surface. In this consideration, a rough surface can be blank PCB laminate; a smooth surface can be distinct types of solder mask or a ceramic substrate.

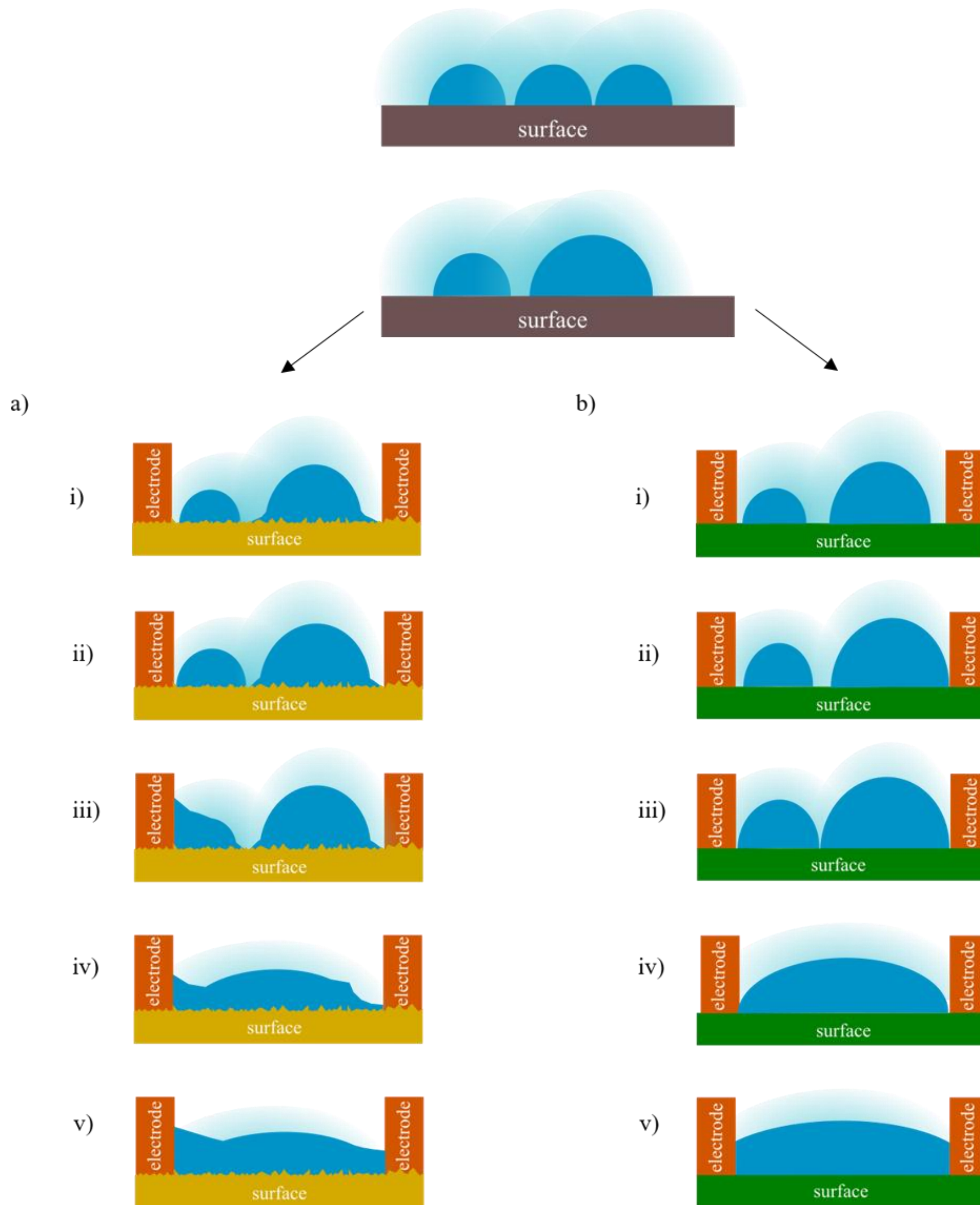


Figure 2.13: Droplet merging into a water bridge between electrodes for rough (a) and smooth (b) surface.

After nucleation of first droplets and their growth, the merging process occurs. Upon fusing, the new droplet contains the volume of the initial droplets, in the considered case, $V_{new} = V_1 + V_2$. When looking at a rough surface with considerable heterogeneity, the surface area is not completely freed upon merging (Figure 2.13a)i)). This is a result of mechanical adhesion when the water is receding. In case of a smooth or hydrophobic surface, the covered surface area is reduced upon merging (Figure 2.13b)i)). Consequently, the greater reduction of surface area for a smooth surface also means that the merged droplet grows more

in height compared to the rough surface. For a PCB surface with closely spaced conduction lines, as condensation proceeds and droplets grow (Figure 2.13ii)-iii)), at some point for the rough surface, there is a point reached when the electrode gap is bridged by a water film of non-uniform height (Figure 2.13a)iv)). Due to the sleekness of a smoother surface, at this time there is no bridging of the gap established yet (Figure 2.13b)iv)). For the rough surface, in the following sequence, the film grows higher and more uniform in thickness (Figure 2.13a)v)). On the smooth surface the eventual film closing across the gap occurs promptly, establishing a bridge of an overall pronounced thickness (Figure 2.13b)v)). The impact of surface nature on condensation has been shown in literature for different scenarios. An elaborate investigation has also been made for solder masks with different roughness in condensation experiments. It was displayed that the rough surface between electrodes was initially bridged sooner. However, by impedance measurement of the patterns over time during condensation, it was shown that once the smooth surface bridged the gap, this resulted in a far more pronounced impedance decrease (Figure 2.14) [6]. This hints to a uniform film of already higher thickness for the rough surface at the time of bridging.

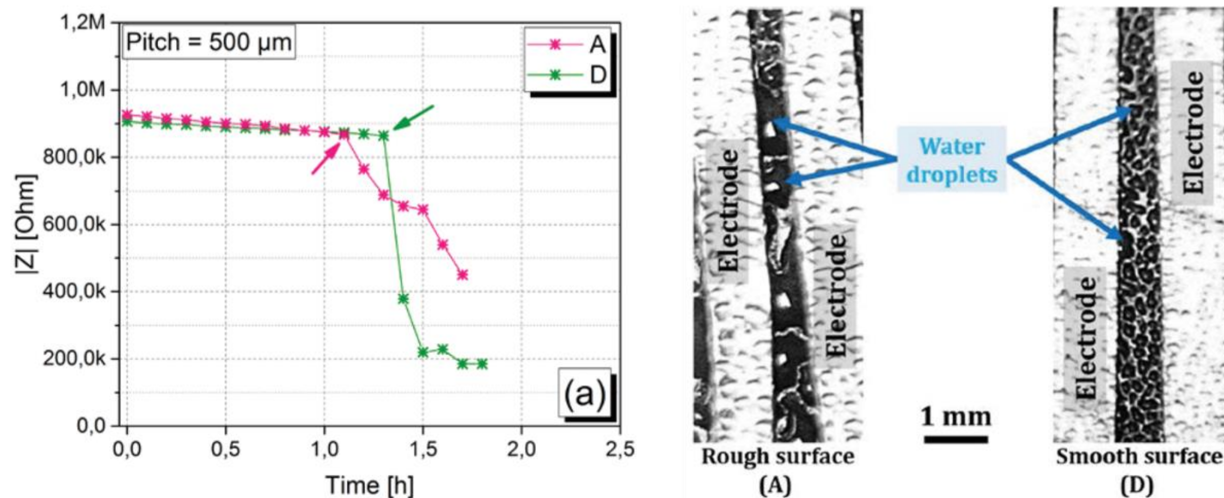


Figure 2.14: Impedance |Z| during the time of condensation experiment for rough solder mask Type A and smooth solder mask Type D along with representative microscope images of the condensation scenarios [6].

Other work has compared FR-4 laminate and polyimide surface in their mean-time-to-condensation (MTTC). The rough FR-4 surface (surface roughness of 2.56 µm) was shown to have a shorter MTTC, supposedly attributed to the possibility of capillary condensation. The smoother Polyimide substrate (surface roughness of 1.69 µm) had an approx. 66 % greater MTTC compared to the FR-4 [5].

The growth rate of condensed droplets has also been investigated on polyolefin substrates with different surface roughness. The variations resulted in differences in droplet nucleation kinetics in a way that the condensation rate for isolated droplets decrease with an increase in surface roughness, water contact angle and contact angle hysteresis (CAH) (Figure 2.15). The influence on volume increase of an isolated drop

was also compared to the volume increase of a drop with neighbors. It was found that the condensation rate was 14 − 40 % lower for the droplet surrounded by others, which blocked the full access of water vapor diffusion [41].

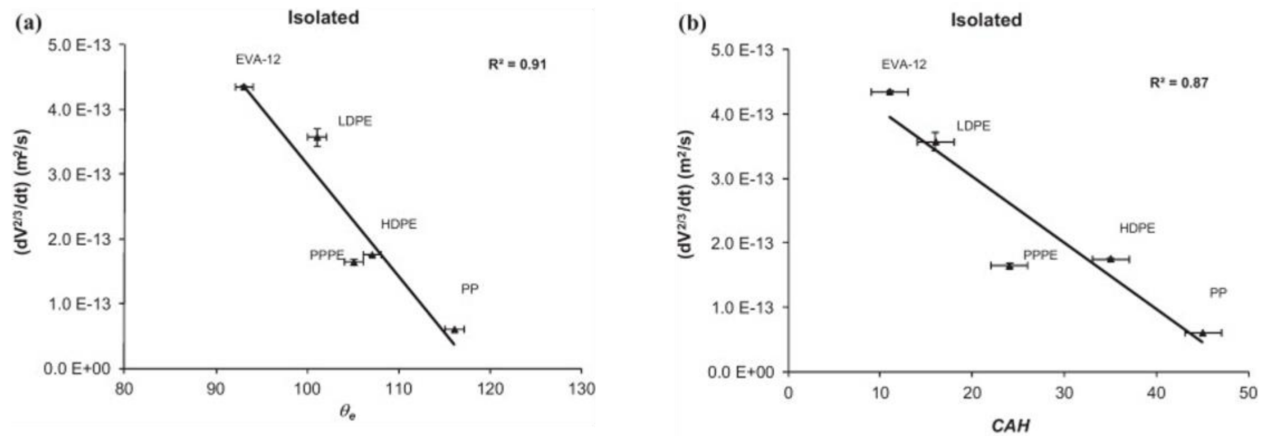


Figure 2.15: Condensation rate ($dV^{2/3}/dt$) as a function of water contact angle (a) and contact angle hysteresis (b) for isolated droplets on five different polymer surfaces (EVA-12, LDPE, HDPE, PPPE and PP) with different surface roughness, adapted from [41].

Edges and corners on a substrate have a significant effect on the water vapor concentration profile over the surface. During condensation, droplets near outer edges tend to grow faster, as they can get more vapor. Droplets at inner edges with worse exposure to the vapor grow slower. Figure 2.16 shows this exemplarily for the condensing behavior on a duralumin surface. For the groove, it can be seen that droplets at the outer edges are of clearly larger size than droplets on the same plane but further away from the edges. In turn, the droplets in the inner edges of the groove are considerably smaller. In the middle of the groove, droplet size is about the same as on the substrate plane away from the edges. The scratch on the surface has a somewhat aligning impact on the droplets but does not greatly influence their size [40].

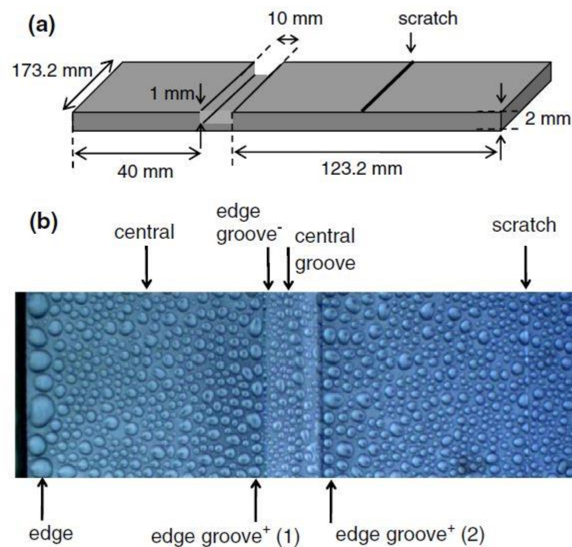


Figure 2.16: Substrate geometries and condensation images with (a) schematic of the substrate and (b) condensation pattern on Duralumin surface [40].

An increase in ambient relative humidity can be associated with a growth in number of monolayers, especially on substrates with non-porous surfaces. A multilayer sorption process can be presumed. Hence, by gravimetric measurements during increase of ambient humidity, a conclusion on the number of absorbed monolayers of water can be made. An example for this approach is shown in Figure 2.17. Thermogravimetric analysis during relative humidity ramp up was determined for an alpha-alumina surface at 23 °C ambient temperature. Based on the assumption of a cross sectional water molecule area of 10.8 Å, at 40 %rH, the first monolayer is built up. From this point on, the growth increases fast with reaching almost 25 monolayers at 98 %rH. A rise in absorbed water has an immediate impact on the surface conductivity [42]. This circumstance and accompanying problems of this increased leak current are further described in Chapter 2.3.2.

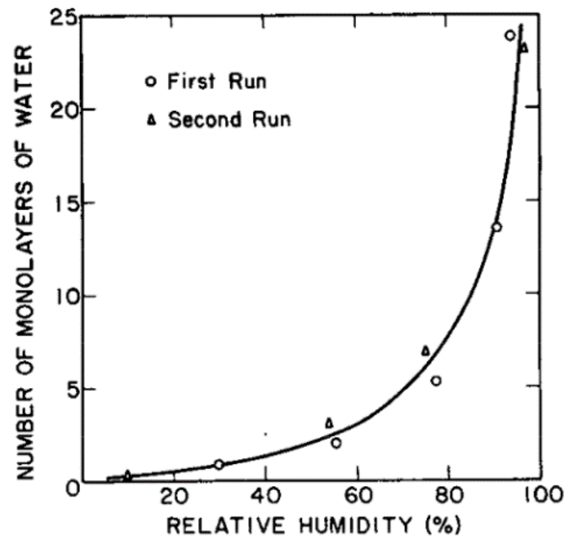


Figure 2.17: Number of monolayers of water depending on relative humidity on an alpha-alumina surface at 23 °C ambient temperature [42].

The formation of a water film from dewing processes is not only dependent on the respective surface properties, but also on the geometrical extension that is considered. This is schematically represented in Figure 2.18. The condensation process starts with small isolated droplets appearing on a surface. Once they grow the merging into larger islands proceeds. Respectively, the probability of droplets coalescing into a water bridge is much more likely for a 100 µm gap than for a 300 µm gap. This is important in the case of PCB surface, as the water layer buildup between adjacent conductors placed with varying separation distance requires different time intervals.

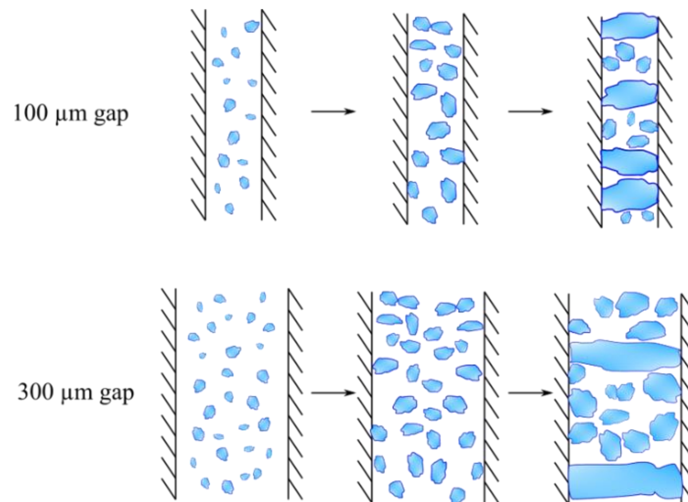


Figure 2.18: Statistical impact on water bridge closing across a small gap (100 µm) and a larger gap (300 µm).

2.2.3 Methods for humidity detection

In the context of humidity detection, there is a wide range of approaches. Humidity sensing is crucial in many fields of industry, such as electronics manufacturing, but also food, pharmaceuticals and chemical production. The conventional approaches employed for humidity detection are illustrated in Figure 2.19. They can be divided into: a) mechanical humidity sensors, b) wet and dry bulb psychrometer, c) capacitive humidity sensors, d) IR optical absorption methods, and e) resistive humidity sensors [43].

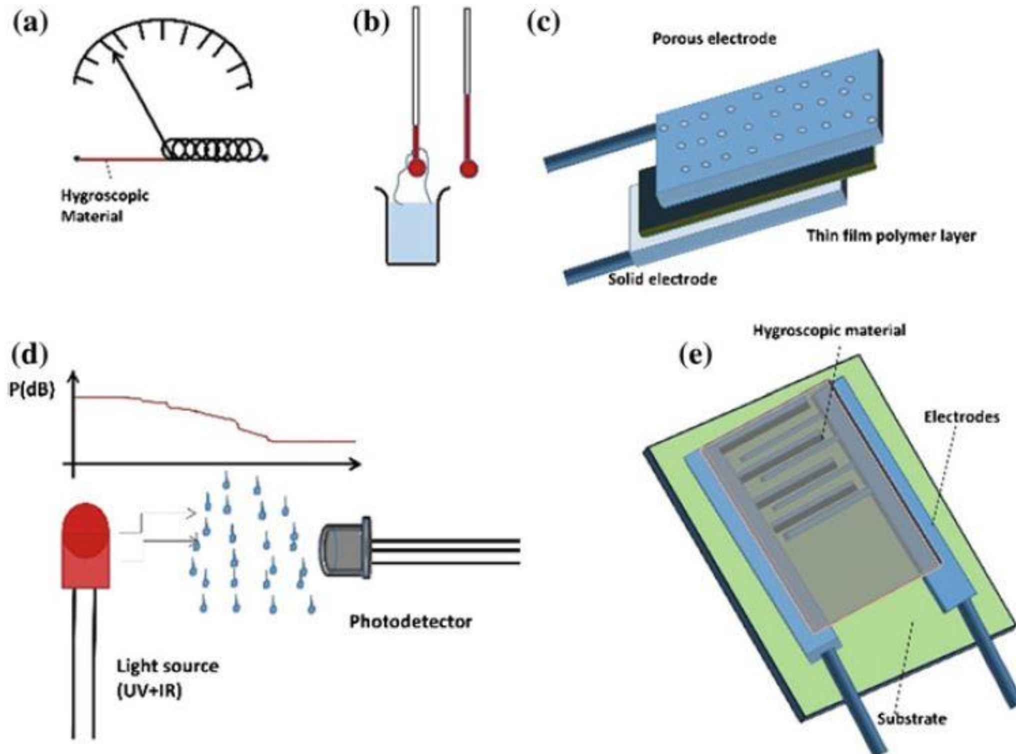


Figure 2.19: Conventional methods for humidity detection. a) mechanical humidity sensor, b) wet and dry bulb psychrometer, c) capacitive humidity sensor, d) IR optical absorption method, e) resistive humidity sensor [43].

Figure 2.19a) represents a mechanical humidity sensor. It relies on the expansion or contraction of a material, relating displacement to a change in humidity. A wet and dry bulb psychrometer (Figure 2.19b)) is based on two thermometers. One of them is the dry bulb, indicating a thermometer that is not affected by air moisture. The other one is covered with a damp wick (wet bulb) and is exposed to the moist air. As moisture is removed from the thermometer surface (evaporative cooling), this cooling impact is measured and compared with the dry bulb temperature to obtain the relative humidity [44]. Both the mechanical method as well as the psychrometer approach are comparably practical in technical simplicity, but they come with the disadvantage of needing elaborate space in the humid air. Capacitive humidity sensors as displayed in Figure 2.19c) represent humidity by changes of dielectric parameters of a thin film upon

humidity sorption or desorption. Among the used materials are polymers, like polyimide (PI), or copolymers based on methacrylates and trimethyl ammonium chlorides [45–47]. The thin film layers are covered with a structured metal electrode that allows humidity penetration of the polymer. Other setup approaches simply place a comb pattern structure on a thin polymer layer to measure interdigital capacitance (Figure 2.20) [46]. The benefit of these sensors is the easy integration into electronics fabrication, as well as the possibility to manufacture them on flexible substrates. However, a disadvantage of these sensor types is the degree of sorption/desorption hysteresis. Consequently, also newly developed materials like graphene oxide are investigated and show promising humidity sensing capacities, with lower hysteresis behavior than conventional materials [48].

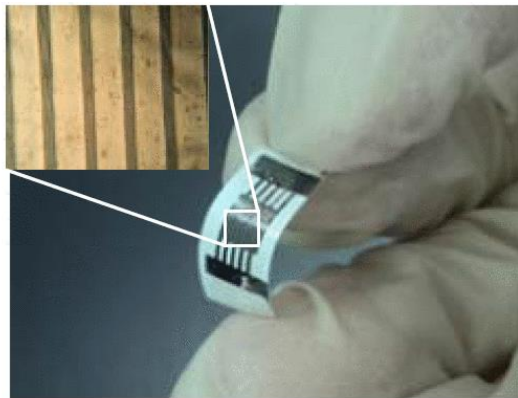


Figure 2.20: Photograph and optical micrograph of a flexible PTFE-PI humidity sensor with aluminum interdigital electrodes [46].

The IR optical absorption method relies on the optical absorption impact of water vapor. As displayed in Figure 2.19d), it measures the transmission of a light emitting source towards a photodetector. Different wavelengths can be used for this approach. Generally, one wavelength with a negligible absorption by water vapor is used as reference and another one with strong dependence of water vapor. By calculating the ratio of the transmission for both wavelengths, a precise measurement of water absorption is possible. The test setting however is limited for the most part to humidity detection in gaseous environments [49].

A resistive humidity sensor (Figure 2.19e)) is - in the same manner as the capacitive sensor - based on an electrical measurement. It rests on humidity induced changes of the resistivity of materials like polymers, semiconductors or composites. Electrical measurement of resistance mostly takes place by an application of a DC-potential across an interdigitated pattern with the humidity sensitive material in between [43]. In a basic approach, a silicon substrate with a metal electrode of Ni, Au or Al can be used and a humidity sensitive layer or PI can be deposited on top [50]. Also new material advancements are used in this area. One example are carbon nanotubes with integrated carboxylic groups on the surface, which result in high humidity sensitivity due to interaction with water molecules via hydrogen bonding. Ambient relative

humidity changes from 20 % to 95 % are reflected in exponential resistance increase. While the general design and measurement concept of the resistive sensor type is relative simple, there are also disadvantages to the method. The major drawback of this sensor principle is considered to be the recovery time, as the humidity requires some time to desorb again from the sensing materials [51].

Other than the mentioned conventional methods, also other techniques can be used for humidity detection. It was shown that it is possible to sense condensate droplets forming in the gate region of a thin film transistor. An InN layer of 1.8 µm thickness acting as gate region and Al-contacts have been used. The sensor current exhibits a decrease by 20 − 30 % within two seconds upon condensation on the InN film (Figure 2.21). The fast sensing mechanism is presumably based on the ion-sensitivity of the field effect transistor. The positively charged donors in the InN layer favor adsorption of water molecules in a way that the oxygen atom is oriented towards the InN surface. Hence, upon condensation, the formation of droplets has a repelling effect on the electrons in surface vicinity. The formation of this depletion zone reduces the sensor current. This sensing mechanism is considered a low-cost approach for different substrates that require fast-response water condensation sensors [52].

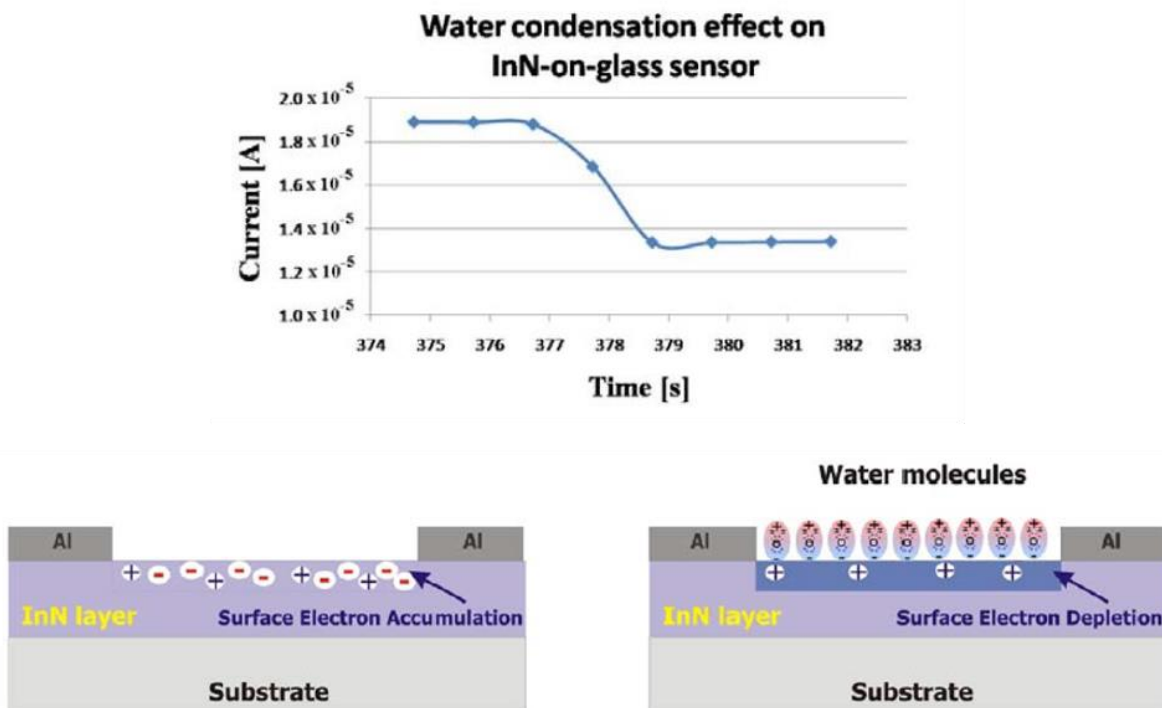


Figure 2.21: Current decrease effect of water condensation on an InN-on-glass sensor and proposed sensing transistor mechanism [52].

Another approach to detect dew condensation is localized surface plasmon resonance (SPR). The method relies on the stimulation of surface plasmon at a metal-analyte interface. The refractive index of the analyte, e.g. water, strongly affects the absorbance and reflectance of the incident light. SPR sensors integrated in nano-scale pores of electronic setups were shown to detect capillary condensation at temperatures higher than the dew point temperature. A potential material is an Au nanocomposite, embedding Au in a thin film of a porous ceramic. The wavelength dependent absorbance changes with condensation, provoked by cooling from 25 °C − 5 °C with the theoretical dew point being at 4.47 °C (Figure 2.22). The increase of broadband absorbance with decreasing temperature is a result of the higher light scattering that comes with proceeding condensation [53]. SPR sensor's advantages of fast response times and non-movable parts are also employed to water-fuel interfaces in order to detect condensation events in fuel tanks [54].

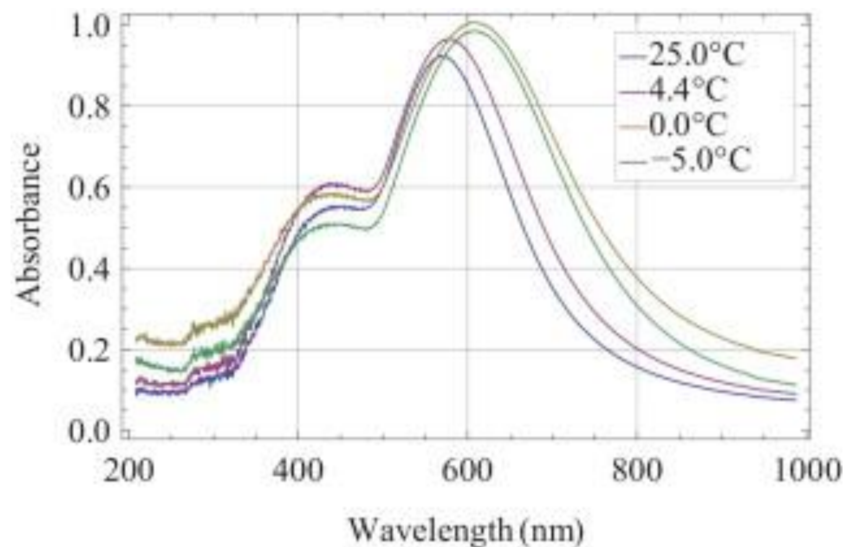


Figure 2.22: Absorbance spectra of an SPR sensor during condensation sensor at temperatures 25 °C, 4.4. °C, 0.0 °C and -5.0 °C in a climatic chamber with ambient temperature of 25 °C and dew point of 4.47 °C [53].

2.3. HUMIDITY RELATED FAILURE MECHANISMS

The malfunctioning mechanisms emphasized in this section put a focus on electrochemical failures that are related to condensation on PCBAs. The VENN-Diagram in Figure 2.23 displays the interplay of the three factors humidity, bias, and ionic contamination that affect electrochemical failures.

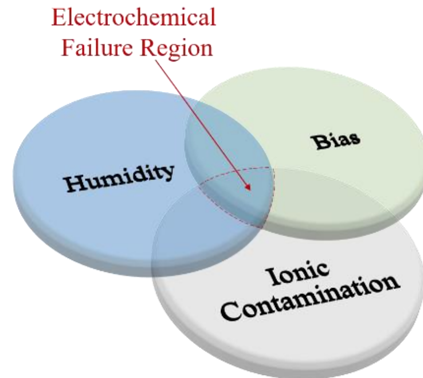


Figure 2.23: VENN-Diagram for illustration of factors that affect electrochemical failures, based on IPC-9201.

Among these factors, the *humidity* can be associated with the end-use environment of a device. Likewise, the *bias* conditions depend on the operating mode of the device and the actual layout, like pitch distances or conductor gaps acting as electrodes and the respective electrical field. Accordingly, the risk that goes along with it is proportional to U/d^2 with U being the potential and d the distance between the electrodes. The presence of *ionic contamination* is greatly influenced by the chosen materials and the manufacturing approach. The contamination is not required for electrochemical failures to occur, but it can accelerate or enhance it.

In the following consideration of electrochemical failures, a differentiation is made between failures that occur in the PCB due to humidity uptake and failures that occur on the PCB surface.

2.3.1 Failures related to humidity uptake of a PCBA

Humidity uptake affecting signal transmission

Moisture in a PCB laminate affects its overall performance, altering thermal, thermomechanical and electrical properties. Relative humidity as well as ambient temperature affect the moisture ingress into the laminate. In order to detect the moisture content in various climatic surroundings, it can be determined as a function of electrical capacitance by attaching metal plates to both sides of a laminate. For a common FR-4 laminate, it was found that independent of temperature between 40 °C and 85 °C, the moisture content increases significantly with relative humidity (Figure 2.24). The capacitive measurement mode with metal foils attached to the laminate supposedly limits the moisture ingress into the laminate, as the metal acts as diffusion barrier. It should therefore be considered that the humidity uptake of blank laminate is even more pronounced [55].

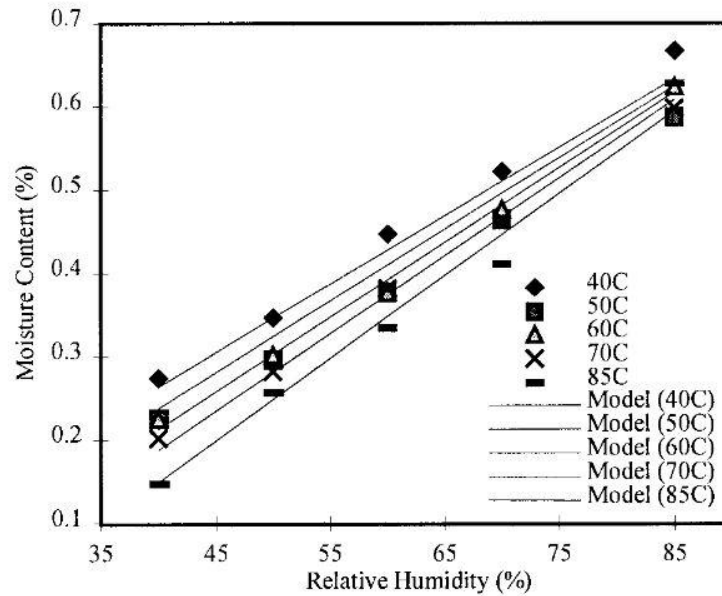


Figure 2.24: Measured and modelled relative humidity dependent moisture content of FR-4 laminate for different ambient temperatures [55].

Aside from electrical measurements giving a percentage, gravimetric experiments confirm the humidity uptake of laminates. The moisture sorption and desorption for exposure to different climatic scenarios is given for different PCB coupons in Figure 2.25. Materials A and C are halogen-free, B and D are halogenated laminates. Moisture gain and loss are based on weight gain and loss and expressed as percentage of the laminate's dry mass. Moisture concentration in the laminates reaches equilibrium for B and C, while still slightly increases until end of test for A and D. Upon drying, all laminates saturate in desorption [56]. Related work also stated that a varying epoxy/glass ratio affects the actual moisture uptake. The diffusion of moisture occurs via the epoxy, without significant absorption impact of the glass fibers, although a weak glass fiber-epoxy interface can be a pathway for moisture transport. Consequently, the glass fabric construction results in different diffusivities, also acting as barrier for moisture intake due to the interface properties [57].

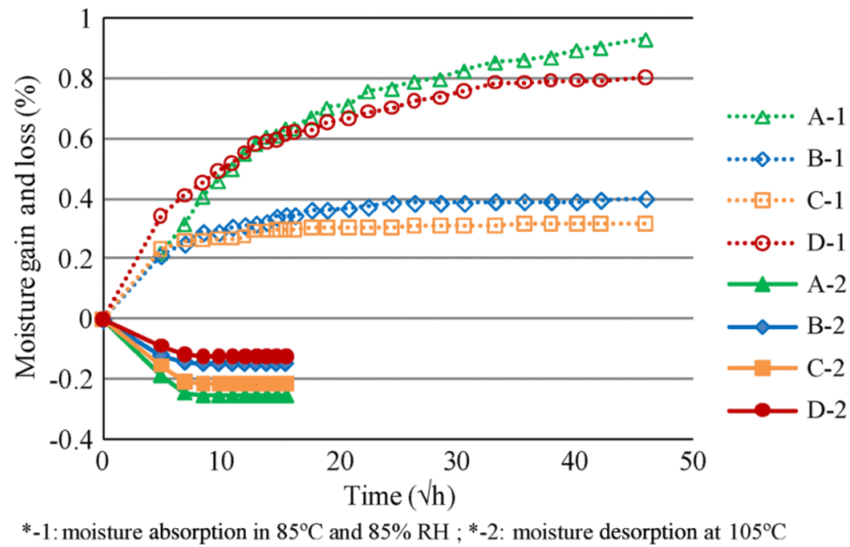


Figure 2.25: Moisture gain and loss measured on each four coupons of four PCB materials (A-D) exposed to 85 °C and 85 %rH (-1) and each two coupons baked at 105 °C in an air-circulating chamber (-2) [56].

The impact of laminate chemistry has also been investigated in another study, comparing different hardening chemistry of FR-4 laminate materials (Figure 2.26). Material C reaches a plateau after approx. ten days at 0.5 % relative mass change, Material A after twelve days at about 0.6 % relative mass change. Material B shows a different behavior with a mass gain about 50 % higher without reaching a saturation until end of test. It differs in hardening chemistry from A and B (phenolic cured epoxy systems), as it uses a dicyandiamide as hardener. The respective introduction of hydrophilic amine groups results in higher amounts of absorbed moisture [58].

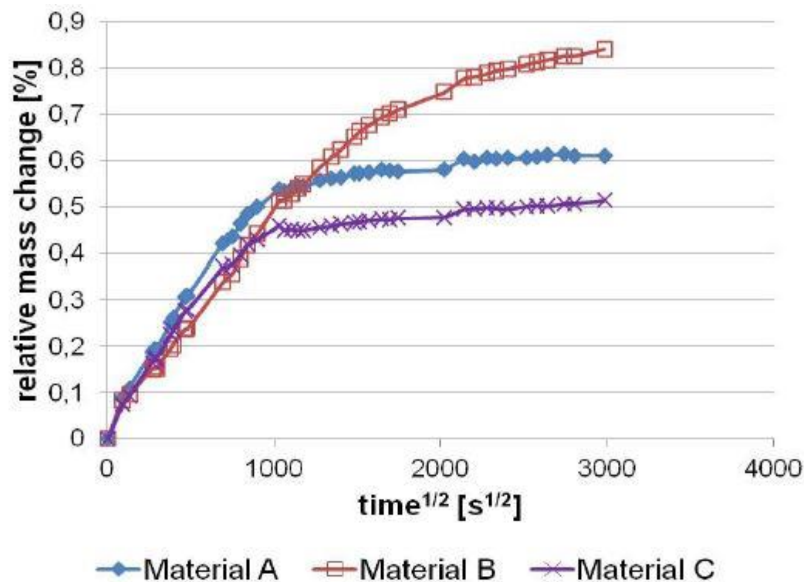


Figure 2.26: Relative mass change of laminate materials due to moisture adsorption at 65 °C and 85 %rH [58].

The uptake of humidity results in changes in dielectric properties of the materials. Figure 2.27 shows an example of the dielectric loss for PTFE and PTFE composites as a function of relative humidity at constant ambient temperature. Especially the composite materials show considerable changes with humidity uptake [59].

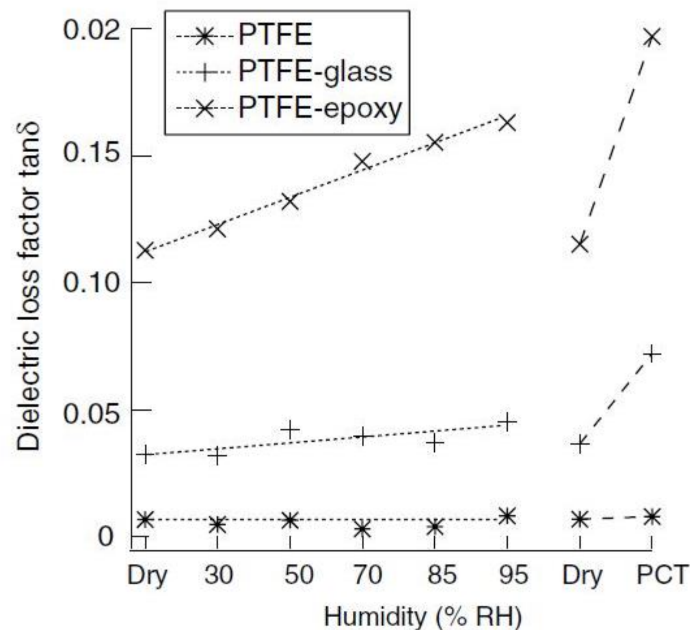


Figure 2.27: Dielectric loss factor of PTFE and PTFE composites obtained at room temperature, respectively at 121 °C and 100 %rH (PCT), adapted from [59].

The consequence of such changes is a direct impact on the performance of signal transfer in inner and outer layers of a PCB. The rapid increase of sensory data in automotive electronics that is pushed by advancements such as autonomous driving requires fast definite signal propagation. Increasingly, higher frequencies in the GHz-region are required to transmit signals via the PCB conductor lines. Humidity induced changes in dielectric properties are consequently a critical issue. Due to the moisture provoked alteration of the laminate, traces may pick up noise from the ambient or crosstalk with other PCB layers can occur [60,61].

Conductive Anodic Filament (CAF)

Aside from failures that are attributed to humidity induced changes in material properties, there is a diverse number of failure mechanisms related to migration phenomena in the context of PCBA electronics. One of the most prominent ones is the occurrence of Conductive Anodic Filament (CAF). It describes the formation of a conductive filament in the PCB base material along the glass fibers. The copper electrodes in between which the filament grows are mostly inner conducting traces or drill holes. In contrast to the conventional

electrochemical migration process, the growth of the filament does not proceed from cathode to anode, but the other way round (Figure 2.28a)) [62]. Figure 2.28b) shows an optical image of CAF between two plated through holes in a PCB [63].

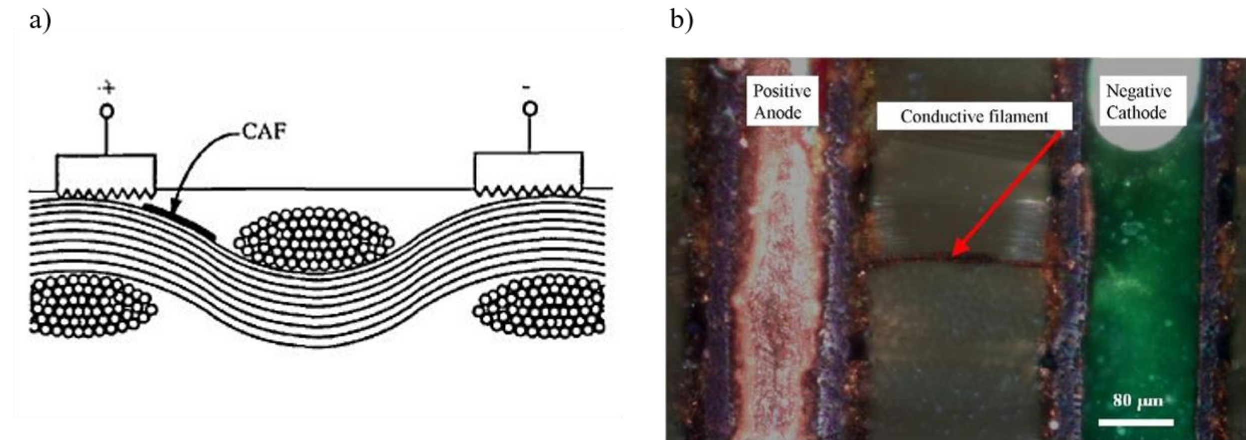


Figure 2.28: a) Schematic representation of CAF bridging two surface tracks from anode to cathode along the glass fibers in the laminate [62]. b) Optical image of a conductive anodic filament between two plated through holes in a PCB [63].

Next to absorbed humidity in the laminate, the reaction process also requires the presence of chloride ions. Chlorine is commonly found as an impurity on PCBAs due to handling issues during manufacturing or external exposure like marine atmosphere. Initiation of the CAF formation is the water uptake of the FR-4, resulting in a weakening of the epoxy-glass fiber interface. This is a rate controlling step for CAF to occur and it is affected greatly by contamination that facilitates moisture diffusion into the laminate [64]. It facilitates water ingress by capillary condensation. The water absorption provides the aqueous medium needed for the electrochemical reaction to occur. Upon voltage application, hydrogen ions form at the anode, accumulate and provide an acidic environment, resulting in the oxidation of copper (Equation 2.6 and Equation 2.7). At the cathode, a reduction takes place, producing OH^- ions (Equation 2.8). This creates an alkaline environment, leading to a pH-gradient between the electrodes.

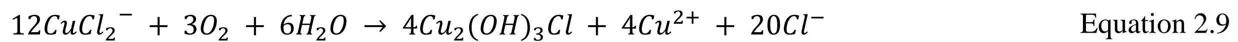
$$H_2O \rightarrow 0.5O_2 + H^+ + 2e^- \quad \text{Equation 2.6}$$

$$Cu \rightarrow Cu^{n+} + ne^- \quad (n = 1, 2) \quad \text{Equation 2.7}$$

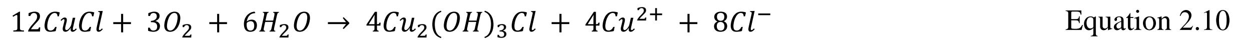
$$H_2O + e^- \rightarrow 0.5H_2 + OH^- \quad \text{Equation 2.8}$$

The subsequent reactions of copper in the chloride environment are not in detail retraced in current state of the art. Different work in this field proposes single step or various two-step reactions that produce $CuCl_2^-$. Eventually, this complex forms the filament. The filament is not of metallic character, but is a $Cu_2(OH)_3Cl$, a copper chloride hydroxyl, also called atacamite, with semiconducting properties [58,65]. The reaction process of the filament occurs according to Equation 2.9 or Equation 2.10. For an environment of very low

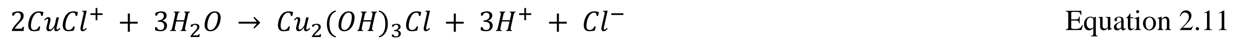
chloride concentration (0.01M - 0.03 M) CuCl dissolves and forms Cu^{2+} ions. In that case, the formation of atacamite can also proceed according to Equation 2.11.



$$12CuCl_2^- + 3O_2 + 6H_2O \rightarrow 4Cu_2(OH)_3Cl + 4Cu^{2+} + 20Cl^- \qquad \text{Equation 2.9}$$



$$12CuCl + 3O_2 + 6H_2O \rightarrow 4Cu_2(OH)_3Cl + 4Cu^{2+} + 8Cl^- \qquad \text{Equation 2.10}$$



$$2CuCl^+ + 3H_2O \rightarrow Cu_2(OH)_3Cl + 3H^+ + Cl^- \qquad \text{Equation 2.11}$$

The atacamite precipitates at the anode as salt and growth continues in direction of the cathode along the electric field lines and the pH-gradient. The semiconducting properties of the $Cu_2(OH)_3Cl$-pathway result in unwanted short circuits. Enhanced leakage currents and false signals entail a failure of the PCBA electronics [65].

2.3.2 Failures related to humidity on a PCBA surface

Considering electrochemical failures on the PCBA surface, various types of corrosion can occur. Some prominent types that are relevant in the context of PCBA electronics are explained in the following.

Galvanic Corrosion

Galvanic corrosion, also referred to as bimetallic corrosion, is a prominent corrosion failure. It is defined as accelerated corrosion of a metal (anode) due to coupling with a more noble metal (cathode) or a nonmetallic conductor in the environment of a conductive electrolyte. This means that three conditions must be met: (i) two metals with a potential difference must be (ii) in electrical contact and (iii) connected by an electrolyte. The electrolyte needs to provide a closed circuit connection between the metals, enabling the redox reaction that destroys the less noble metal (Figure 2.29). The strongest corrosive impact is at the interface of both metals and decreases with distance to the junction [66].

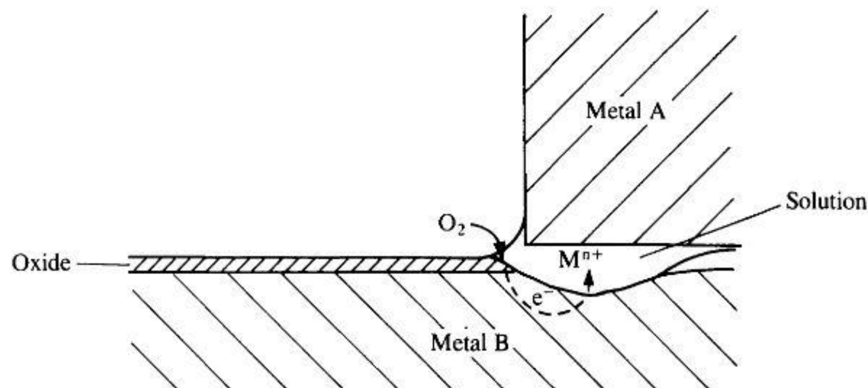


Figure 2.29: Schematic representation of galvanic corrosion with metal B being less noble than metal A [66].

The standard reversible potentials are commonly used to assess the risk of galvanic corrosion in metal coupling. Generally, their positioning in the galvanic series provides a prediction about whether the less noble materials is destroyed by the redox reaction. The difference of corrosion potential in the series however, is not the only determining impact on the extent of corrosion. Galvanic corrosion was shown to occur for metals with a potential difference of only 50 mV, whereas coupling of metals with as much as 800 mV can remain corrosion-free. This is because the kinetics of corrosion depend on the current flowing, which in turn is dependent on various other factors like the precipitating electrochemical reactions, the actual anodic and cathodic surface areas and the electrolytic solution properties [67–70].

On a PCBA, galvanic corrosion can occur when gold and underlying electroless nickel are coupled or also between a copper layer and an ENIG surface finish contact. An example is shown in Figure 2.30a) for a mobile key pad. The schematic setup of the layers is shown in Figure 2.30b). The Scanning Electron Microscopy (SEM) image in Figure 2.30c) shows the corrosion of nickel and the underlying copper. This can occur due to porosity and imperfections of the gold layer, presumably due to manufacturing problems (Figure 2.30d)). The large difference of standard electrode potential for gold and nickel (Figure 2.30e)) results in the gold acting as efficient cathode, and causing corrosion of the electroless nickel layer. Proceeding corrosion can even lead to the exposure of the underlying copper, which is then no longer protected from corrosion [68,71].

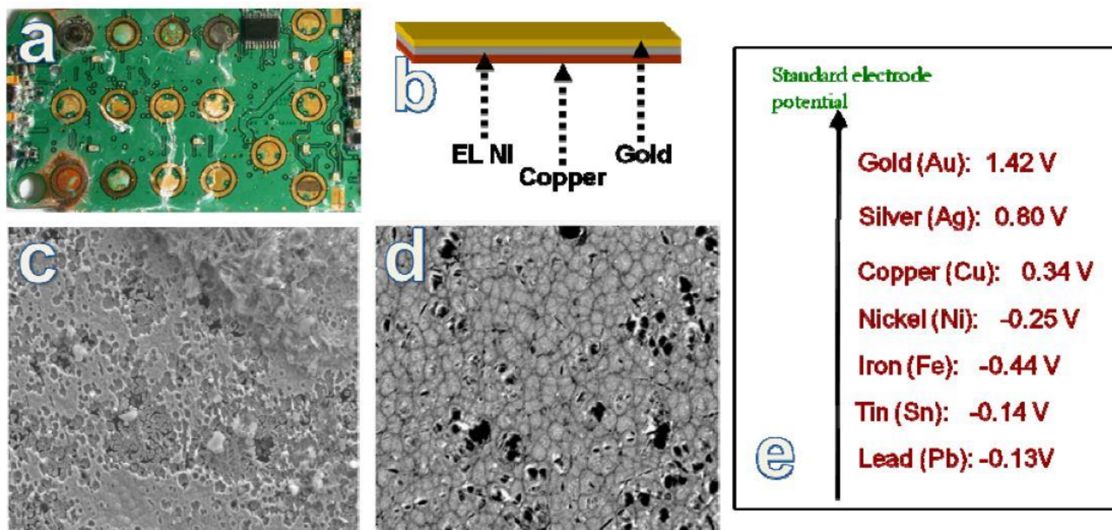


Figure 2.30: a) Mobile phone pad showing galvanic corrosion. b) Schematic setup of the copper, electroless nickel (EL NI) and immersion gold layer. c) SEM images of nickel and underlying copper. d) SEM images of porous gold layer exposing the EL NI layer. e) Standard potential listing [68].

The area of anode and cathode has considerable effect on the severity of corrosion. This is because charge balance should be possible to establish during the corrosion process. Therefore the charge produced by one

electrode should be consumed by the other electrode. Thus, the anodic and cathodic currents need to be considered equal. This results in Equation 2.12, signifying that the product of relative cathodic surface area S_c and current density i_c equals the one of relative anodic surface area S_a and current density i_a.

$$i_a = i_c \frac{S_c}{S_a} \qquad \text{Equation 2.12}$$

A large cathode area compared to anode area equals that more oxygen reduction is possible, hence the galvanic current rises and the corrosion level increases.

Galvanic corrosion can be prevented by measures like adequate materials selection, insulating the parts of the metal couple from each other or using cathode/anode surface area ratios $\frac{S_c}{S_a}$ much smaller than one [69,70].

Creep Corrosion

Another known corrosion mechanism in the PCBA context is creep corrosion. It describes the corrosion of copper or silver metallization on the PCB and the creep of the resulting corrosion products in a way that they form unwanted electric shorts between different PCBA features. Especially when copper is exposed to environments of water and high sulfur contents, soluble salts will form. Once they become mobile, they can creep between conductor lines or component terminals, causing electrical malfunction. The impact of surface finish on the creep corrosion susceptibility has become prominent upon the restriction of hazardous substances (RoHS) legislation in Europe. The consequent banning of the traditional SnPb HASL finish has led to usage of alternatives like OSP, ENIG or ImAg [72,73]. It was found in the tests under sulfur and chlorine atmosphere that both OSP and ImAg finished PCBs showed creep corrosion in the low relative humidity range up to approx. 50 %rH. ENIG finishes however showed creep corrosion in low and high relative humidity ambient (Figure 2.31) [74].

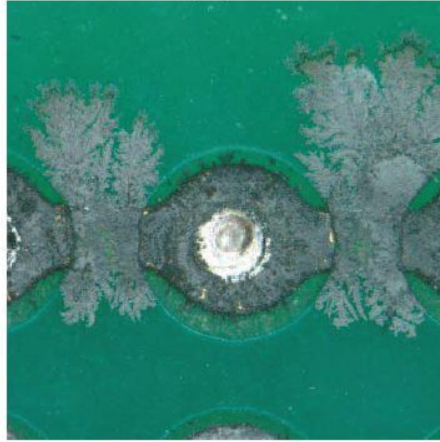


Figure 2.31: Example of creep corrosion between plated through hole pads with exposed copper and ENIG finish after exposure to 74-80 %rH [74].

Corrosive gases can accelerate creep corrosion. Electronics are found in the environment of aggressive gases in many industrial sites, for example in food industry or in marine territory. These gases promote interaction of moisture layers and metal surfaces by (i) assisting the formation of moisture layers by formation of hygroscopic particulates, (ii) controlling the pH of moisture layers and (iii) governing the dissolution of oxide layers and promoting ligand exchange [67]. A variety of organic and inorganic gases such as chlorine, sulfur-containing compounds or nitrogen-containing compounds consequently have a severe impact on the durability of electronics. For an electronic power module with silver conducting lines long-time exposure to sulfur containing gases was shown to result in various types of corrosion. Silver sulfide corrosion was prominent uniformly on all of the silver surfaces of the ceramic substrate. In addition, the formation of sulfur compounds in relation to silver migration and creep corrosion at the gold-wire silver interface of the circuit occurred. The reaction process of the silver sulfide corrosion, leading to acanthite (Ag_2S) is given in Equation 2.13. The corrosion process is sped up by presence of water, however does not depend on it being present [75,76].

$$2Ag + HS^- \rightarrow Ag_2S + 0.5H_2 \qquad \text{Equation 2.13}$$

<u>Leakage Current / SIR</u>

An initial buildup of surface water has a direct impact on surface conductivity. Figure 2.32a) shows the conduction current for an alpha-alumina substrate as a function of the relative humidity and the number of water monolayers. With 10^{-14} Å to 10^{-11}Å, the leak current is in a very small range, but it still mirrors the number increase of only a few monolayers. The conductivity even at 98 %rH is still an order of a magnitude lower than that of bulk water. It can therefore be assumed that the leak current only passes through connected patches, which in cross-sectional consideration is only a fraction of a continuous water film [42]. Other work aiming at the surface conductivity of water layers adsorbed to solids has investigated the impact

of different relative humidity for Teflon and quartz surfaces. Conductivity was based on current measurement at 30 V (Figure 2.32b)) It was related to number of absorbed water layers, obtained by gravimetric measurement under the assumption of monolayer adsorption uniform across the samples. The quartz surface is generally more affected by the humidity increase. Conductivity increases exponentially with number of layers, after the first monolayer is established. Teflon however does not show any changes in conductivity increase after completion of the first monolayer. Hence, the surface conductivity is strongly dependent on when the water molecules become mobile. For Teflon, the interaction of the molecules with the surface is so small, that there is a generally higher mobility from the beginning on, while for the quartz that is only given after buildup of at least one layer [77].

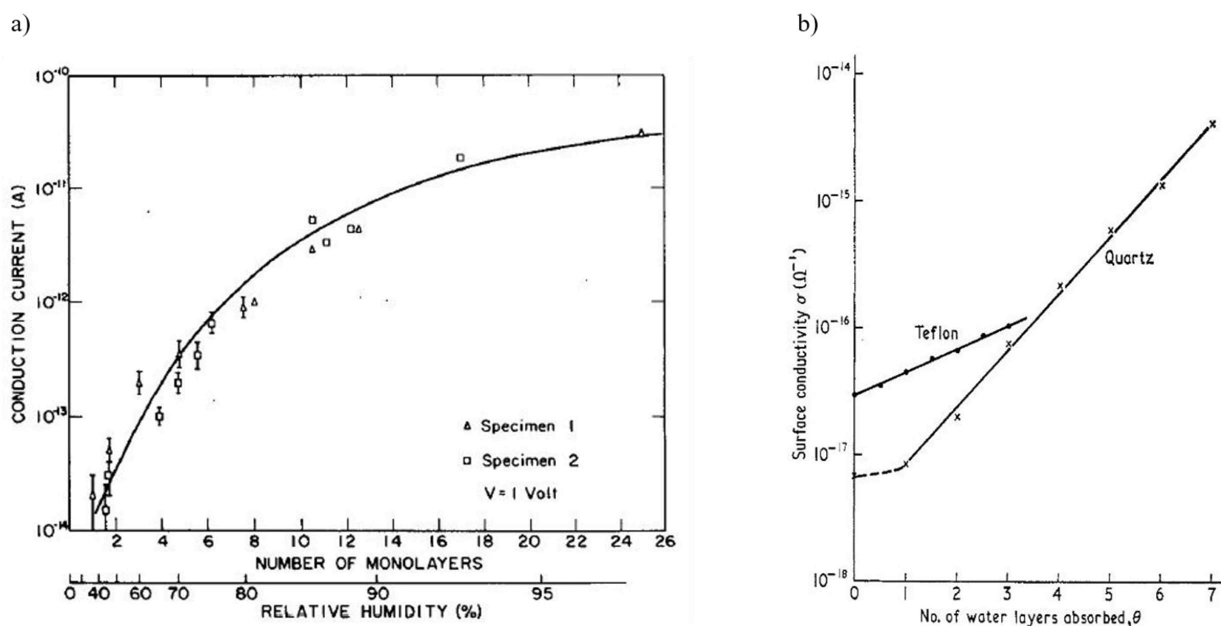


Figure 2.32: a) Conduction current upon application of 1 V as a function of monolayer number on the alpha alumina substrate in the given relative humidity ambient [42]. b) Change in surface conductivity for Teflon and Quartz as a function of number of absorbed water layers at 23 °C [77].

Increase of leakage current above a distinct threshold parameter can result in electrical breakdown of the electronic assembly. Failure of electronic circuitries due to short formation or non-proper signal transmission are common failure causes. Assessment of such failures are commonly evaluated by changes in surface insulation resistance. According to the standard IPC-9201, surface insulation resistance (SIR) is defined as property a material and electrode system. It can be considered as sheet resistance, but is also affected by bulk conductivity, leakage current through electrolytic contaminants, multiple dielectrics or metallization materials and also air as a medium [78]. Consequently, four possible routes in principle determine the leakage current across the surface between two conductors (Figure 2.33). These are (1) through the gas phase, (2) via contamination on the surface, (3) along the surface and (4) through the

substrate [79]. Essentially, condensation can greatly decrease the leakage current across the surface. At an ambient relative humidity of > 50 %rH, some monolayers of water will be present on the surface. With increasing number of water monolayers and transition into multilayer setup, the conductivity between two electrodes rises.

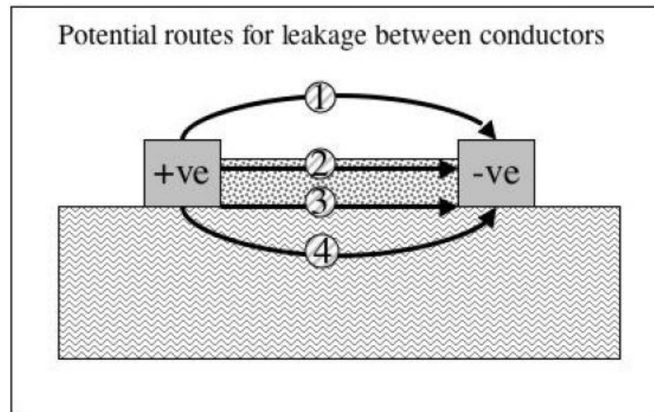


Figure 2.33: Four potential leakage current routes between conductors. (1) gas phase, (2) surface contamination, (3) surface, (4) substrate [79].

Leakage current via the surface depends strongly on the surface properties. Figure 2.34 shows the impact of four different surface finishes on the SIR-value on a PCB with weak organic acid (WOA) flux residue. Solely the type of the finishing layer affects the SIR by various orders of magnitude [80]. This needs to be considered when equating a distinct leakage current threshold with the occurrence of an electrical failure of a setup.

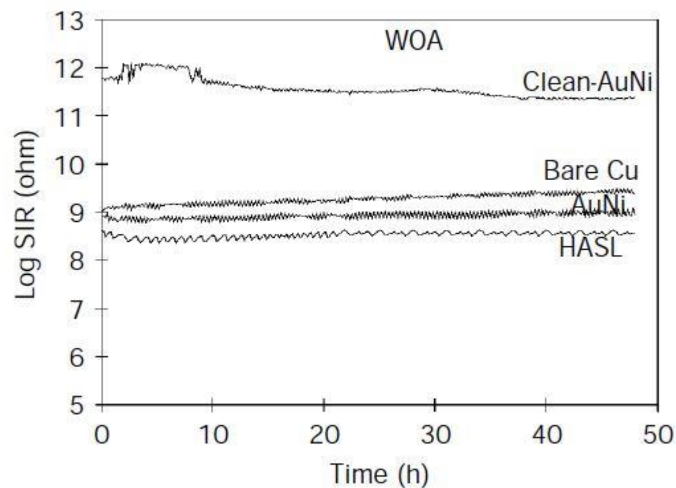


Figure 2.34: Impact of four different surface finishes on the SIR value of a comb pattern test board with weak organic acid (WOA) flux at 65 °C and 85 %rH for 5 V DC [80].

Measurement of leakage current progression over the course of time can identify short circuit formation between electric contacts due to corrosion. Respective current progression is exemplarily shown in Figure 2.35 on bipolar transistor samples. Several Devices under Test (DUT) were tested at 85 °C and 85 %rH for approx. 5000 hours. Until 1700 hours, currents remain at a low level, only showing noise. Afterwards they increase by several orders of magnitude (individual DUT failures times indicated in green, black and blue) Subsequent analysis confirmed corrosion of the aluminum metallization [81].

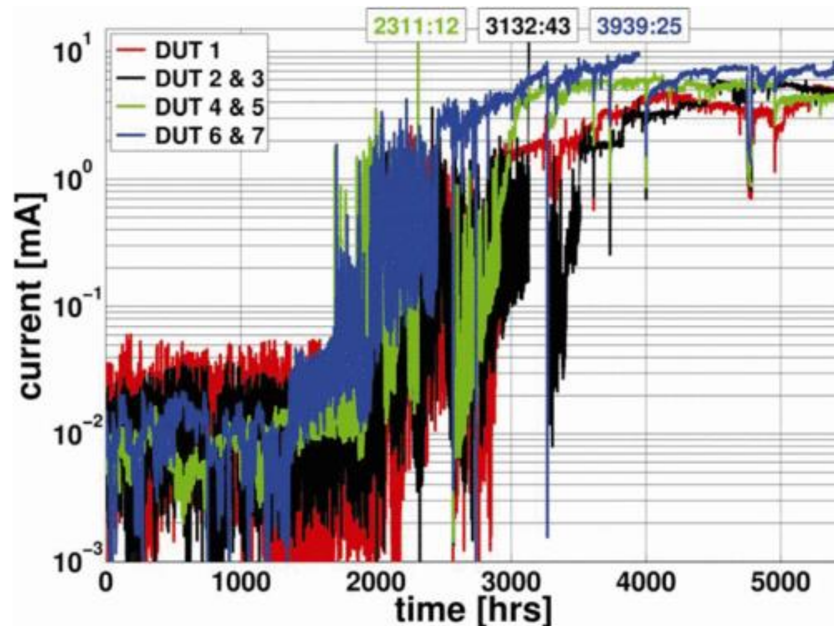


Figure 2.35: Leakage current monitoring for transistor DUTs at 85 °C and 85 %rH ambient conditions [81].

An increase in leakage current can be provoked by ionic contamination. With dissolved ions, the conductive electrolyte forming reduces the overall SIR [79]. Figure 2.36 shows an overview of the surface conductivity measured for different compounds on Printed Wiring Boards (PWBs). It can be seen that a combination of adipic acid and polyethylene glycol (PEG 400) has the same impact on surface conductivity as NaCl [82].

Surface Conductivity for PWBs with Surface Deposits

Compound	*Amount Deposited* (μg/cm²)*	*Surface Conductivity (mho)*	*Critical RH (%)*
NaCl	2.00	1.3×10^{-8}	76
NaF	1.44	4.0×10^{-11}	97
NaBr	3.52	3.8×10^{-11}	84
KCl	2.55	3.1×10^{-11}	84
$MgCl_2$	1.63	2.9×10^{-8}	44
$CaCl_2$	1.90	9.5×10^{-8}	29
HCl	1.25	2.4×10^{-10}	($CuCl_2$:82)
Succinic acid	4.04	9.2×10^{-11}	98
Malic acid	4.59	3.3×10^{-11}	86
Glutaric acid	4.52	3.9×10^{-11}	84
Adipic acid	5.00	2.7×10^{-11}	99.6
PEG 400	13.70	3.2×10^{-10}	0
Adipic Acid + PEG 400	5.00 + 13.70	1.4×10^{-8}	
Blank	0.00	3.5×10^{-11}	

* All deposited values correspond to the molar-ionic equivalent of 2.0 μg/cm² NaCl.

Figure 2.36: DC Surface conductivity measured at 35 °C and 90 %rH for surface deposits of different chemical compounds on interdigitated Cu patterns on FR-4 [82].

The most prominent contaminant reducing SIR in the PCBA context is flux residue [83–85]. The flux residues lead to reduced SIR in two ways: (i) due to their hygroscopic characteristics, they generally enforce condensation on the PCB surface. (ii) Once they dissolve in the condensed water film, they enhance its conductivity once more, facilitating corrosive processes. The higher current values due to flux contamination have a direct impact on corrosion reliability and respectively field reliability of electronics [86].

Potential leak current routes through the gas phase can be considered negligible for conventional PCBA setups. However, air discharge can be relevant for high voltage DC testing. Breakdown characteristics for kV-DC-pulses become a more prominent topic with trends towards higher integration density and more complex logic circuits [87].

When detecting increased leak currents in a test or field scenario, it needs to be considered that a respective failure can be only temporary. An elevated current level can be attributed solely to localized condensation events. These do not necessarily result in actual corrosive failures, if other essential preconditions like voltage thresholds or a distinct amount of time are not given. In other cases, increased leak current levels can be due to actual corrosion failures like corrosion products that short-circuit two different metal poles. However, also these failures modes can be of transient character only, for example due to burning of short

circuit connections once high leakage current run through them. This hampers a subsequent correlation, as tracing of an actual physical failure after a test and establishment of a root-cause relationship is not always possible. This matter is often referred to as “trouble not identified” (TNI) or “no trouble found” (NTF) [88].

Electrochemical Migration (ECM)

One of the most common failures related to formation of a thin water layer on the PCB surface is the formation of an electrically conductive dendrite between supposedly isolating parts of a circuit. Temporary or permanent establishment of an unwanted short circuit can lead to malfunctioning of the electronic setup. The basis for dendrite formation is the process of Electrochemical Migration (ECM). It describes the growth of a metallic filament on a PCB through an aqueous electrolyte under application of a DC potential bias between two oppositely biased metal electrodes. The single process steps can be retraced in detail based on Figure 2.37. The requirement for ECM to occur is the formation of an electrolyte path between anode and cathode. Electrodissolution can take place, meaning metal ions are created at the anode and immerse in the electrolyte. Under the DC electrical field, the ions are transported to the cathode, where they are reduced and deposit, forming the dendrite. If this process can proceed long enough, the dendrite can grow back to the anode and create an electric short between the two poles [89,90].

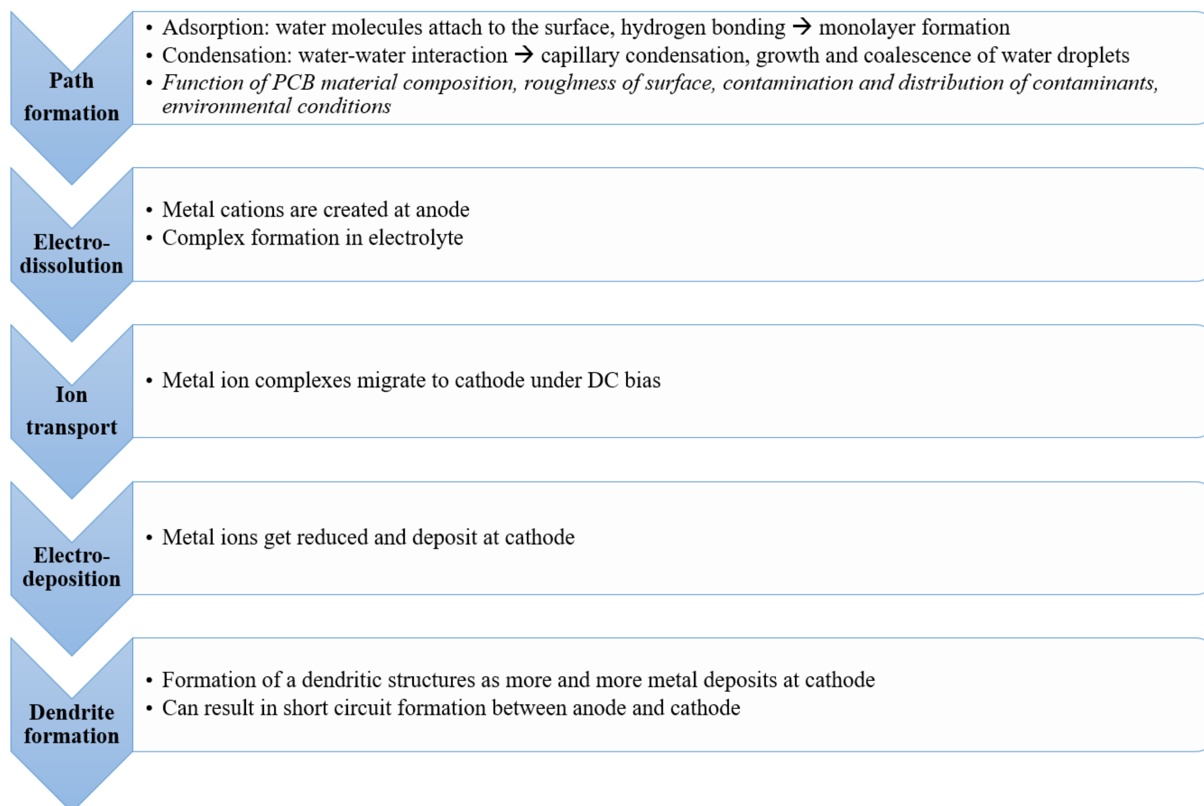


Figure 2.37: Subsequent steps of the ECM failure phenomenon.

In detail, the ECM process is schematically represented in Figure 2.38, along with the depicting the involved chemical species. At the anode oxidation and metal dissolution take place. This involves production of hydronium ions (Equation 2.14) and the electrolytic dissolution of the metal electrode (Equation 2.15), which can be copper, for instance (Equation 2.7).

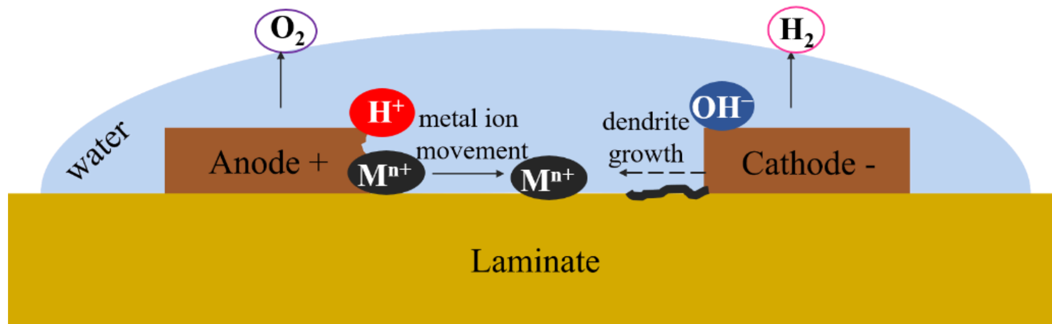


Figure 2.38: Schematic representation of ECM and dendrite growth on a PCB surface.

$$H_2O \rightarrow 0.5O_2 \uparrow + 2H^+ + 2e^- \quad \text{Equation 2.14}$$

$$M \rightarrow M^{n+} + ne^- \quad \text{Equation 2.15}$$

At the cathode, the reduction process and starting dendrite growth occur. Hydroxide ions are produced (Equation 2.16) and the metal is reduced and precipitates (Equation 2.17) [91].

$$2H_2O + 2e^- \rightarrow H_2 \uparrow + 2OH^- \quad \text{Equation 2.16}$$

$$M^{n+} + ne^- \rightarrow M \quad \text{Equation 2.17}$$

ECM can occur for various metals, besides the mentioned copper it is known to appear for silver, tin, tin-based solder with varying silver or copper composition as well as lead [92–97]. Figure 2.39 shows ECM resulting in growth of copper (a) and tin (b) dendritic structures. The tree shaped structures result from the fact that the deposition of metal ions occurs primarily at the tips of the growing dendrite, as the electrical field strength at those points is at a maximum.

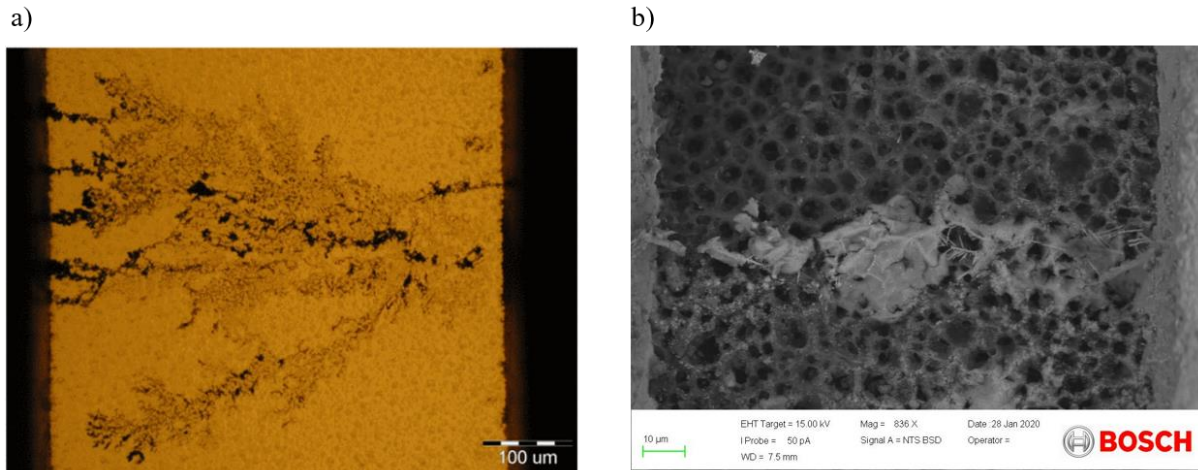


Figure 2.39: a) Copper dendrites caused by ECM [98]. b) Tin dendrite provoked by application of a 10 V DC potential across a 125 µm gap between tin terminals on FR-4 laminate during condensing conditions.

Aside from the cumulative conditions of a DC bias promoting the electrochemical reactions and an electrolyte allowing the ion transport, the kinetics and severity of the ECM process in detail are affected by various factors. The ECM risk is in the first instance dependent on the solubility product of the electrode metal. The migration rates of the solubility products for different metal ion hydroxides have been shown to correlate well with temperature-humidity-bias test's mean-time-to-failure (MTTF). In Figure 2.40, this relation is depicted for silver, lead, copper and tin. It is explained by supposing a diffusion controlled deposition at the cathode, meaning the speed depends on the metal ion concentration in the electrolyte and the hydroxide precipitate formation impacts the maximum metal concentration in the electrolyte through the solubility product. This relationship is only correct however, if no additional ionic contamination is present [99].

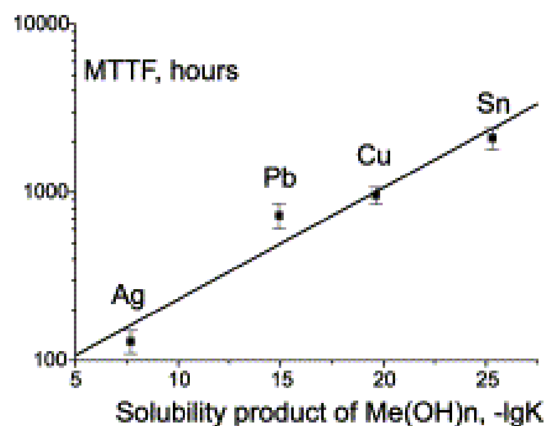


Figure 2.40: Solubility Product of Ag, Pb, Cu and Sn in a THB test associated with mean time to failure (MTTF) [99].

Another impact factor is the characteristic of the surface between anode and cathode. Figure 2.41a) shows results of a water drop (WD) and a Temperature Humidity Bias (THB) test for FR-4 substrate and for polyimide (PI) substrate. Different MTTD (equaling mean time to dendrite growth) showed that in THB tests, FR-4 samples failed sooner. Comparing with the water droplet (WD) test that showed no significant difference in MTFF, this was identified to be due to the condensation effect. Mean-time-to-condensation (MTTC) is longer for PI, being attributed to the fact that it is less porous than the FR-4. FR-4 has a considerably larger effective surface area, with higher surface energy, and accordingly it is prone to pore condensation. Thus, the electrolyte path formation as initial boundary condition for ECM has a considerable impact on the kinetics of failure occurrence [5]. The applied potential, hence the strength of the electrical field driving the reactions also affects the ECM process. The probability for dendrite shorting rises with field strength, meaning with higher voltages (U) across a distinct gap size (d). Higher field strength results in higher ion migration speed. Different sources postulate an ECM-correlation with U/d or U/d^2 [100]. Figure 2.41b) displays the increasing ECM-probability for increasing U/d^2. However it was also shown that this relationship is an interplay of different factors and for some spacing ranges, spacing can be a more relevant factor on ECM than the overall electric field [101]. It must me however be considered that also in this regard, the mentioned gap sized dependence of time to water-bridging needs to be taken into account.

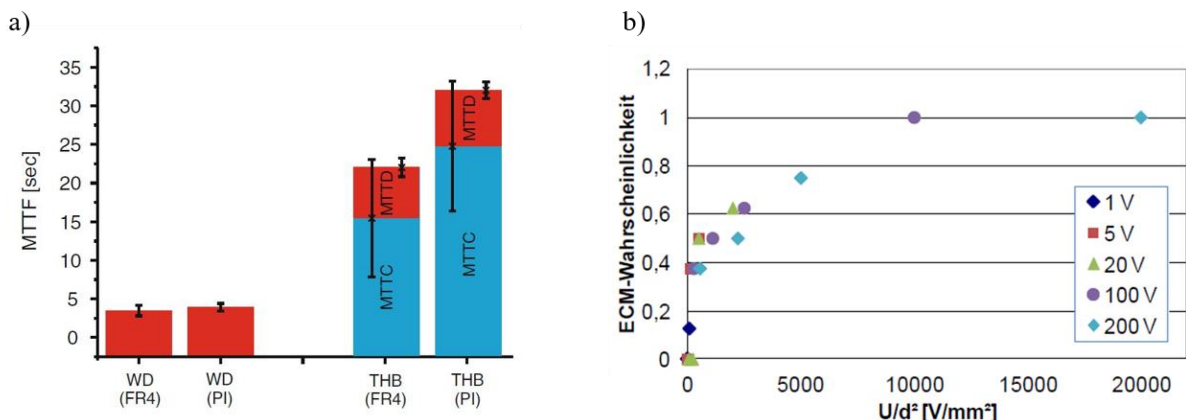


Figure 2.41: a) Mean-time-to-dendrite (MTTD) and mean-time-to-condensation (MTTC) for 200 µm gap comb patterns on FR-4 and Polyimide (PI) substrates in water drop (WD) test and Thermal Humidity Bias (THB) test [5]. b) Impact of U/d^2 on the ECM-probability (ECM-Wahrscheinlichkeit) for 70-85 °C/85-90 %rH with flux residues on test patterns [100].

The ECM-impact of contamination, for example from the PCBA manufacturing process, has been subject to various studies [84,102–106]. Contamination can have an impact on ECM in two ways, depending on its properties. Firstly, if it is a hygroscopic contaminant, it facilitates water film formation on the surface and thus contributes in providing a pathway for the ECM process. Secondly, if the contamination is ionic, it improves conductivity of the electrolyte. It increases the solubility of the metal as it provides the necessary

ligands to form metal complexes. Thus, ionic contamination is generally considered to enhance the ECM risk as the resistivity of a surface contaminated with hygroscopic compounds decreases drastically at a point where the compound critical relative humidity is reached. However, not only ionic contamination has an impact on an absorbed water film. Compounds like polyglycols or other types of organic surfactants that come to use in flux systems can be hygroscopic. Even though they do not affect conductivity of an adsorbed water film, they still increase the thickness of the film. This way, they provide a dissolving medium even for contaminants with low hygroscopy that could otherwise be considered harmless at low relative humidity [78,107]. Contamination like chlorides were demonstrated to enhance water film formation and dendrite growth between pure copper terminals and between tin-plated terminals of SMT chip capacitors [84,108]. The ECM-occurrence can be retraced by measurement of leakage current, exemplarily shown in Figure 2.42. The dendrites formed between copper electrodes on FR-4 are shown for two different levels of chloride ion concentration (a) contamination with 0.1 mM NaCl, b) with 1 mM NaCl) in a thin electrolyte layer across the electrodes. The leakage current measured shows that ECM-susceptibility increases with increased chloride concentration. The ionic conductivity of the electrolyte is enhanced by the contaminant. It accelerates the anodic dissolution of the copper and the cathodic deposition process [108].

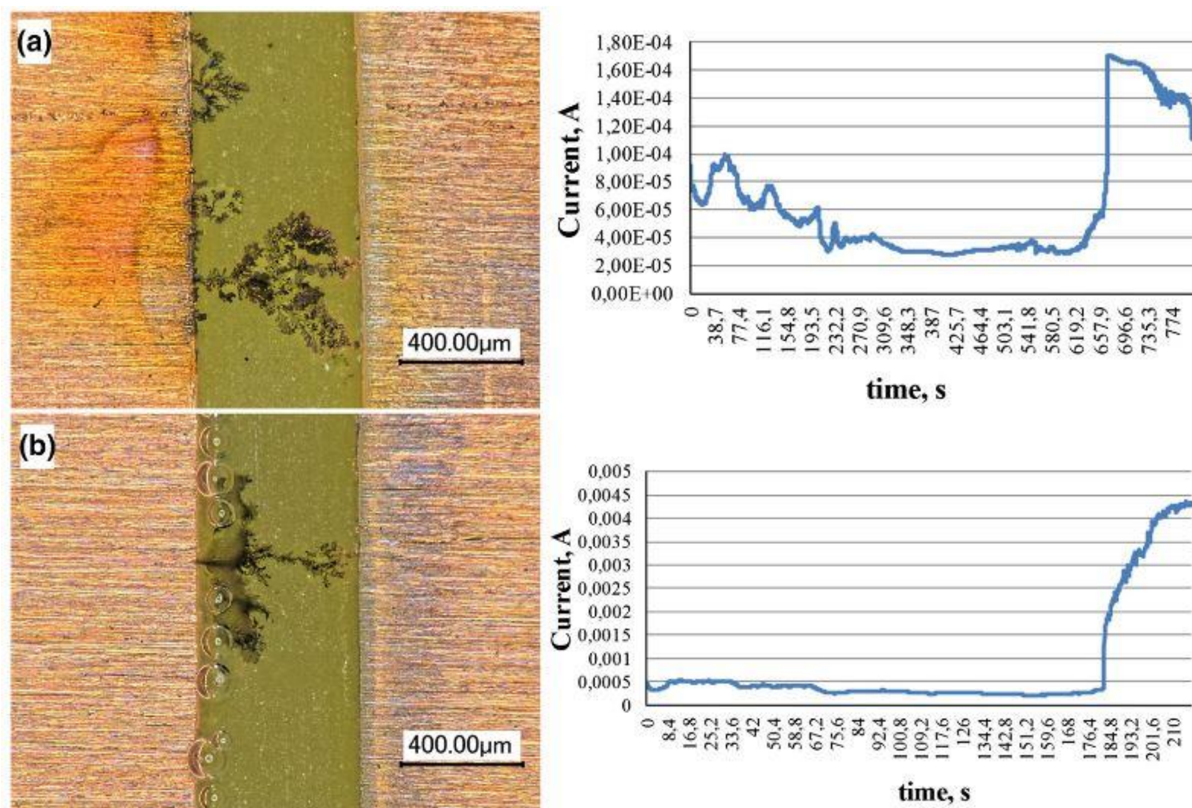


Figure 2.42: Optical micrographs and leakage current progression after thin-electrolyte-layer testing with (a) 0.1 mM NaCl concentration and (b) 1 mM NaCl concentration [108].

Solder fluxes, especially no-clean flux systems as used in reflow soldering and other PCBA soldering processes are a well-known source for contamination. In case of the nowadays-used no-clean solder pastes, the flux residue is supposed to decompose during soldering and not leave corrosion critical residues accessible for reaction. However, a complete removal or encapsulation cannot be granted [86]. In terms of corrosion enhancement, especially weak organic acids (WOAs), acting as activators are regarded critical. They are of hygroscopic nature and consequently enhance adsorption of ambient moisture [3,24]. Various studies have tested different flux residues with regard to their ECM-susceptibility [85,109,110]. For instance, glutaric acid is known to considerably enhance dendrite growth, having a lower deliquescence point than for example adipic or succinic acid. When glutaric acid is applied to a PCB-test board with interdigital electrodes, leakage current measurements display corrosion appearance with increasing relative humidity. In Figure 2.43a), the applied glutaric acid has been dried at room temperature. In Figure 2.43b), the PCB has been heated after application and consequently the acid was partially removed. The lesser WOA-amount is mirrored in the current progression. Dendritic shorting reflected in current increase only occurs at 99 %rH. For the non-heated specimen, the electrodes are shortened by dendrites already at 80 %rH [3].

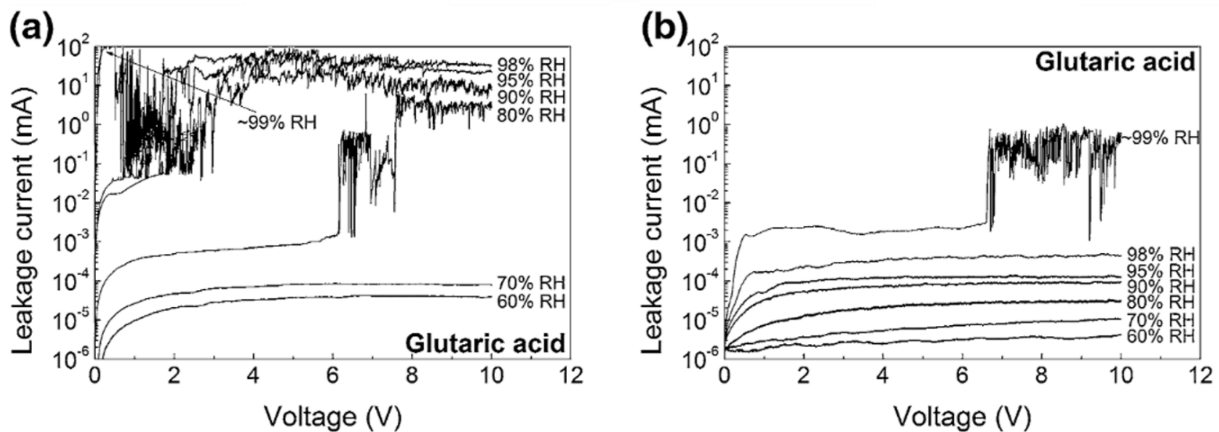


Figure 2.43: Leakage current for applied voltage on PCB comb pattern pre-contaminated with glutaric acid (100 µg/cm^2) and dried at (a) room temperature and (b) at 220 °C to 245 °C for 45 s, measured at 25 °C and humidity levels from 60 %rH to 99 %rH [3].

The occurrence of dendrites can in some very rare cases also result from AC application instead of a DC bias. This phenomenon however is rarely researched according to literature [111]. Nonetheless, for the known cases, the migration phenomenon is triggered only by a very low frequency. As a results of the low frequency, for a limited amount of time, the two involved electrodes can be considered as anode and cathode. Within the time-frame of an AC-half cycle, an oxidation reaction at the then-anode can take place. Due to inertia, the produced ions do not fully migrate back to the electrode within the opposite AC-half

cycle. This can eventually result in net-migration of ions to the cathode and hence to ECM. The appearance of dendritic structures under AC bias has been shown for copper electrodes at frequencies ≤ 10 Hz and a DC offset of 2 V [7,112].

2.4. CLIMATIC RELIABILITY TESTING

Reliability of electronic setups in various climatic scenarios is a key element to be considered in the development and manufacturing process. The conception procedure of original electronic equipment at the Robert Bosch GmbH is displayed exemplified for a control unit in Figure 2.44. It can be segmented in technology development, product development, and manufacturing of the original equipment. In technology development, the first approach is to conduct physico-chemical tests on sample patterns and carry out simulations if procurable. Materials that are qualified accordingly can be released for product development. In this development stages, complete platforms are tested in series like conditions. Hence, the risk analysis for different failure mechanisms is established. Basis for this are usually testing methods and setups that are codified in international standards, for example test methods for ionic analysis and cleanliness [113,114]. In the next step, specific customer requirements are included in the setup. In this process, it is often required to adapt the PCBA setup if failures occur and then repeat testing with slight changes in design (referred to as B-sample, C-sample etc.). After conclusion of these preliminary tests, the series product needs to be released at the end of the product development process. In manufacturing of the product in plants, regular process monitoring and audits are carried out to ensure compliance of all processes according to formalized regulations.

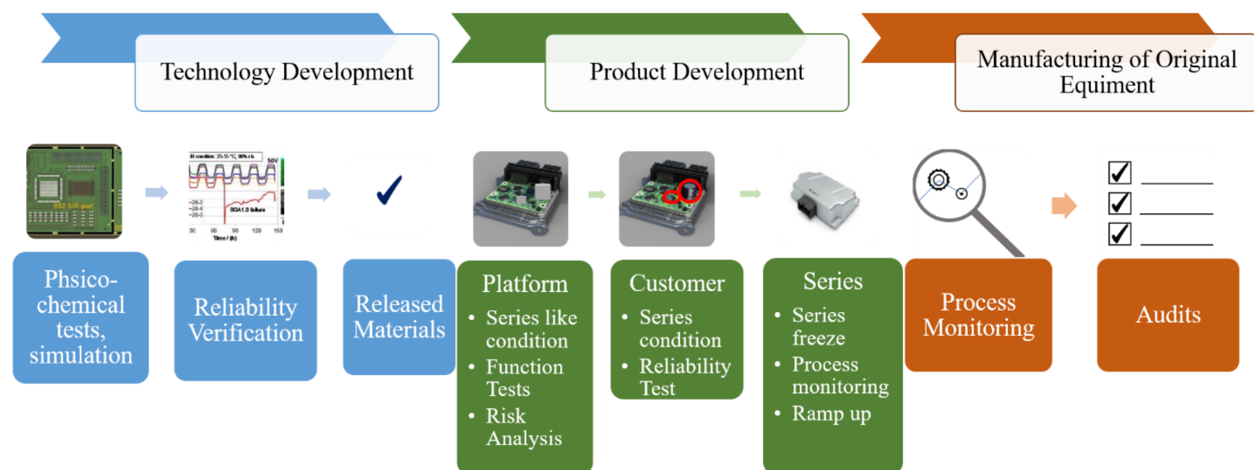


Figure 2.44: Product development stages with reliability relevant sub-items. Pictures in Technology and Product Development obtained from [14,115].

Testing procedures during technology and product development involve various characterization methods. These include stability under mechanical loads like vibration or shock, electrical testing like Surface Insulation Resistance, partially related to reliability in distinct climatic scenarios [116]. Accordingly, testing involves assessment of quality capability for various failure reasons. In technology development, these impact factors are evaluated for simplified test setups, in order to recognize critical configurations early on. In product development, released materials from technology development are evaluated once again, but in a more complex PCBA setup. So generally, the validation process includes various sequences of testing approaches for different PCBA-groups. A test protocol for a C-sample validation as one of the last processes in product development includes for example various repeating test runs of cyclic temperature (-40 °C − 105 °C), optical inspection, electrical testing at room temperature and temperature and humidity bias (85 °C and 85 %rH). To approach humidity robustness of the final product, it is apparent that in all levels of development, respective tests need to be conducted. Considering the VENN diagram (Figure 2.23) of the impact factors “humidity”, “bias” and “ionic contamination” for electrochemical failure occurrence, it is apparent that careful material selection at an early stage, as well as combined loads of humidity and bias in a more complex PCBA stage need to be taken into account for appropriate product design. All conducted tests are lastly based on accelerated aging, being approximated to the product performance degradation over lifetime. This involves the application of stress like temperature, voltage or mechanical loads with greater severity compared to actual field environment. Several pitfalls need to be minded with this approach. Among them are causing failure modes that would not be observed under standard operating conditions like chemical processes induced by high temperatures or non-consideration of the uncertainty of statistical estimates [117]. Added to that is the fact that electronic assemblies like PCBAs are becoming increasingly complex. More materials are involved, integration density is continuously higher and novel design concepts come to use [118,119]. As a result, the number of field returns is increasing. This indicates that there is a gap in testing for reliability requirements and actual field conditions of the devices. Likewise, it demonstrates that there is a number of failure mechanisms, which are not understood during development or not tested in appropriate manner [120]. In the following, two methods that can be used to assess electrochemical failures of a PCBA are described. The Surface Insulation Resistance (SIR) method is a conventionally used approach to evaluate humidity related failure mechanisms in a PCB. The test is commonly utilized in material and product release processes in electronics development. Electrochemical Impedance Spectroscopy (EIS) is a measurement technique that studies the complex response of a system perturbed by an alternating current. Via the impedance response, the system can be characterized. The method is not applied in a standardized form for ECM-reliability assessment in automotive electronics development. However, it is a well established analysis technique in fundamental scientific research and specifically in the area of humidity induced electronics failure, it has proved its general capability.

2.4.1 Surface Insulation Resistance (SIR) method

The SIR method is widely used in electronic industries. It typically qualifies processability and durability of PCB-setups with regard to humidity robustness. Basis of the measurement is the application of a DC potential to a specimen in a distinct ambient climate. The measured leakage current is represented as an insulation resistance that indicates changes in bulk or surface resistivity if electrochemical processes occur under humidity influence (as described in Leak Current Failure in Chapter 2.3.2). In process or material qualification, the experimental tests are executed based on different industry standards [78,79,121]. These differ in climatic surrounding, duration, voltage classes that are applied to the specimen, or other characteristics, exemplarily shown for two standardized tests in Table 2-2 [122,123].

Table 2-2: Overview of characteristic for standards describing SIR tests [122,123].

Standard	IPC-TM-650, 2.6.3.7. J-STD-004B	IPC-TM-650 2.6.14.1
Ambient climate	40 °C / 90 %rH	40 °C / 93 %rH 65 °C / 88.5 %rH 85 °C / 88.5 %rH
Duration	168 h	500 h
Voltage Class	5 V or 25 V/mm	100 V
Pass Criteria	SIR > 10^8 Ohm	No visual evidence of ECM failure

A variation of test parameters has an impact on the initial SIR value of a test pattern in non-condensing condition. With increasing test voltage, the SIR slightly increases likewise (Figure 2.45a)). The respectively increasing electric field results in potential ion movement on the insulting surface towards the electrodes. This supposedly generates a depletion region in between that increases the SIR. Likewise, relative ambient humidity affects the SIR value. Figure 2.45b) shows the fall in SIR for patterns with two different levels of salt concentration (KI), mimicking contaminants left on the PCBA after manufacturing, for a rise in relative humidity. Generally, an increase in relative humidity entails in a higher number of absorbed water layers to the surface. This results in improved mobility for the K^+ and I^- ions, hence in SIR-drop. For a higher salt concentration (Figure 2.45b) open circle) the water molecules in the ambient have more ions available for absorptive interaction and higher conductivity of the forming thin electrolyte layer. Thus, the SIR is lower at all times, compared to smaller salt concentration. Accordingly, in planning and interpretation of an SIR test for reliability studies, impact parameters on the sensitivity of the method need to be considered [121].

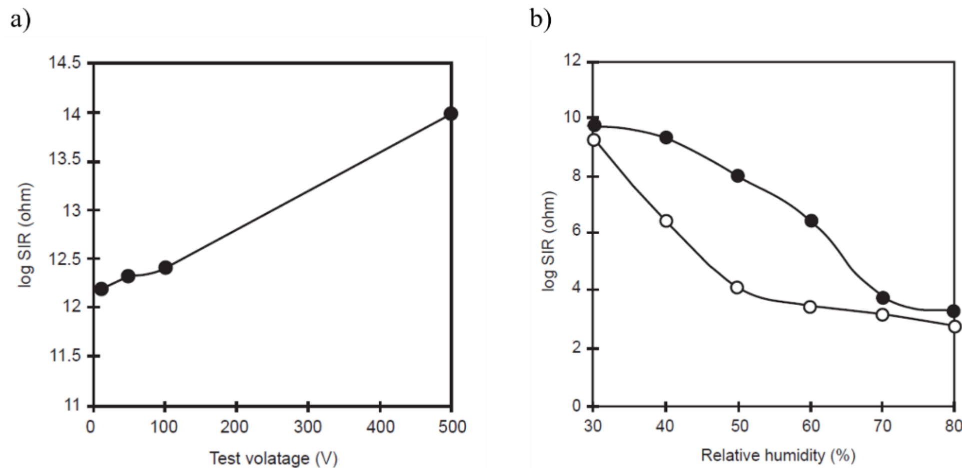
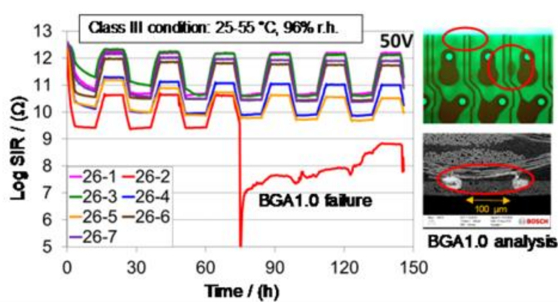


Figure 2.45: a) Impact of applied voltage on SIR-value. b) Impact of relative humidity on SIR-value with filled circle for a KI salt concentration of 300 µg/square inch and open circle for a KI salt concentration of 1000 µg/square inch, test voltage 100 V [121].

For an SIR test to allow a reliability assessment of a PCBA, it is crucial to replicate actual product designs. For that, special coupons are developed to be used as test specimen, partially also described in the standards. They are supposed to match in design the actual sizes used in an electronic product. This is often done by testing on interdigital metallized comb patterns of different gap sizes or by measurement in between the poles of SMD-components. This way, basic material reliability as for solder pastes or coatings can be evaluated but also potential risk factors like trapped flux residues below components after soldering can be simulated [124]. Figure 2.46a) shows measurement results of a SIR-test conducted on advanced developed "B52 test board" according to IPC-9202. The board includes - amongst others - dummy test components like BGA1.0, QFN0.5 as well as capped SIR-comb patterns under SMD-capacitors. A cyclic heat damp SIR-test (following IEC 60068-2-30) with 6 cycles of 25-55 °C at 96 %rH and 50 V DC bias was conducted to assess an advanced solder paste and process qualification. In this particular case, the results indicate that all tested parts are considered non-critical as they remain above the determined 10^8 Ohm SIR-limit. The only exception was the BGA1.0 that showed ECM failures (SIR-drop after approx. 75 h). Accordingly, the SIR heat damp cyclic test reliably determined ECM-critical conditions [115]. Figure 2.46b) displays exemplary results of a coated and an uncoated solderpaste comb pattern, tested at 40 °C and 90 %rH with 12.5 V DC bias for 220 hours. Even though both board types showed no signs of electrochemical migration and the SIR values remained above critical limits, the humidity-sealing attributes of the coating are represented in the SIR values [125].

(a) SIR data for test patterns on an advanced B52 test board



(b) SIR data for two solder paste comb patterns with and without coating

Figure 2.46: a) Assembled B52 advanced test board and SIR data with 25-55 °C, 96 %rH cyclic condition, 26-1 – 26-7 refer to different patterns on the B52 test board [115]. b) SIR values for two solderpaste-comb patterns with coating and without coating, 24 hours and 220 hours into an SIR test at 40 °C/90 %rH [125].

SIR tests are considered a rapid method for comprehensive testing scenarios in PCBA quality. However, various studies show that a careful consideration of measurement values is needed to classify ECM-criticality by means of the technique. Potential pseudo-failures in testing require extensive analysis of patterns after testing in order to ensure that a critical SIR actually hints to corrosion criticality. Two examples representing this need are shown in Figure 2.47. Figure 2.47a) shows SIR data of three IPC-B-25 based comb patterns with 6.25-, 12.5- and 25 mil spacing (corresponds to 0.16, 0.32 and 0.64 mm), coated with SnPb solder. The patterns were additionally coated with a urethane conformal coating. The data for all patterns with applied 6 DC Bias under 40 °C and 93 %rH environment shows a reliable progression with values > 10^8 Ohm for the 6.25- and the 25 mil gap. The 12.5 mil in-between size however shows a sudden SIR-drop after approx. 130 hours, rising to a stable value again shortly after. Analysis after testing revealed that the pattern was contaminated with a fiber that supposedly led to temporal drop below the 10^8 Ohm failure criteria [90]. Thus, after subsequent analysis, all sample configuration could be considered non-critical in terms of corrosion, even though the SIR data was initially alarming. A similar case, however even more problematic, in terms of analysis is depicted in Figure 2.47b). SIR-data for seven comb patterns of 100 µm gap coated with SAC-based solder paste are shown for a 1000 hours test at 40 °C and 90 %rH and 100 V DC. All curves eventually drop below the 10^8 Ohm threshold, indicating a test failure of the patterns. The following optical analysis of the patterns showed however that only some of the electrical breakdowns could be attributed to corrosion (e.g. Ch06, green). Other specimen showed no signs of ECM but instead fiber contamination was found on the pattern (Ch03, blue). The issue with pseudo failures partially nullifies the generally easy and convenient SIR-measurement approach. An encompassing evaluation of electronics reliability in a distinct climate cannot solely rely on the electrical test data.

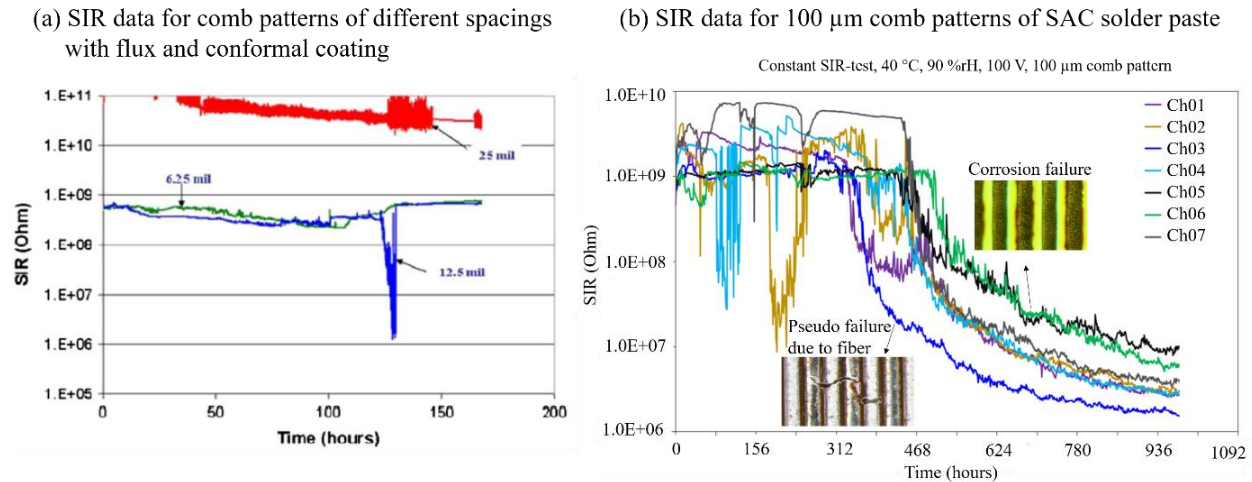


Figure 2.47: a) SIR data obtained for deactivated rosin-based flux with urethane conformal coating in 40 °C/93 %rH ambient and 6 VDC bias for spacings of 0.64 mm (25 mil, red), 0.32 mm (12.5 mil, blue) and 0.16 mm (6.25 mil, green) [90]. b) Exemplary data of 1000 hours constant SIR-test with 40 °C/90 rH on 100 µm gap comb patterns with SACbased solder paste. SIR reduces over the course of time for all patterns, however subsequent analysis shows only corrosion relation for some patterns (eg. Ch06), while other classify as pseudo failures (Ch03).

Various other studies report the unsatisfactory knowledge gain of failure-cause relationships with SIR measurements. The SIR value is often considered an indicator for (in-) sufficient circuit isolation. When used as a control measure for corrosion enhancing contaminants, it is able to detect the presence of significant contamination. However, the mobility of ions or a precise contaminant impact on corrosion cannot be assessed unobstructed [7,126]. Correspondingly, an SIR test does not necessarily deliver more information than testing methods like ROSE (Resistivity of Solvent Extract) or Ion Chromatography analysis. These techniques are simply used to detect the presence of ionic contamination on boards, but cannot relate the presence to an actual failure occurrence [127]. Although in comparison with these approaches, the SIR test delivers a statement on the corrosive consequences of the ions present, none of the methods is able to assess an overall information on the whole picture of steps leading up to the failure and the failure itself. Some studies also state that the electrical pass/failure criteria of SIR like 10^8 Ohm are partially unsuitable for detecting ECM or CAF failure. If the short-circuiting structures burn right away due to the high DC voltage application, these short events can get lost in periodical data recording [128]. Detailed durability information, for example when wanting to distinguish the residue level of soldered capacitors covered with conformal coating is also only conditionally possible with SIR testing. Different levels of cleanliness were not clearly distinguishable by an SIR test in high humidity and temperature ambient [129]. To counteract these issues that come with the SIR method, knowledge about the dependencies of SIR values are crucial, such is regular monitoring of the specimen during test. Pass/fail criteria such as regulated climate scenarios of official standards are therefore to be considered with caution as well [130].

2.4.2 Electrochemical Impedance Spectroscopy (EIS) method

Electrochemical Impedance Spectroscopy (EIS) is a measurement approach that relies on the application of a small alternating voltage signal (ΔE, mV-range) to a system under test (Figure 2.48). A broad band of frequencies can be used, going from mHz to GHz. The response of the system to the alternating excitation is a function of the complex impedance Z of the system. Depending on the system's properties, the input signal can also be shifted in phase (φ).

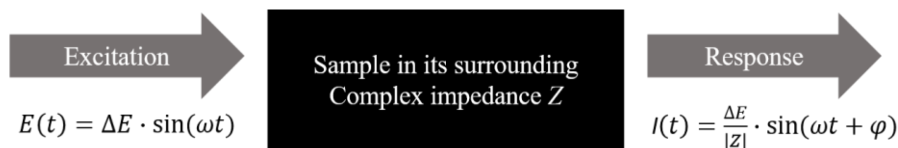


Figure 2.48: Schematic representation of EIS technique with excitation of the system by an AC voltage ΔE for an angular frequency ω and the system's response, affected by $/Z/$ and phase shifted by γ.

The representation of measurement data can be conducted by a Nyquist Plot, showing the real part *Re* (also referred to as Z') and the imaginary part *Im* (Z'') for the used frequencies. An alternative is the Bode Plot representation, giving the impedance Z of the system and the phase shift (usually designated by either φ or Φ) for the scanned frequency range [131,132].

The application of an AC signal with a frequency input results in the corresponding response of the system for the applied frequency. If the system has capacitive or inductive properties, these can be assessed via the phase shift towards the excitation signal. The resistive parts are primarily affected by the area of the electrodes, their distance, and the specific resistance of the medium between them. The capacitive parts depend on the permittivity of the system. For low frequencies close to DC status, capacitive parameters behave highly resistive, while for higher frequencies the capacitances are more prominent. Conductive parameters show the reversed dependence, showing a higher impedance with increasing frequency. The interpretation of EIS data is often performed by relating the experimental data to an electrical equivalent circuit. Due to the capability of the EIS method to represent resistive, capacitive, as well as inductive and mixed-property elements of a system, the data can be modelled accordingly. Some frequently used components and their impedances are listed in Table 2-3. Added to the standard components resistor, capacitor, and inductor are the Constant Phase Element (CPE) and the Warburg Impedance. The CPE represents an imperfect capacitor that displays a certain frequency dispersion. In case of $\alpha = 1$, it is a purely capacitive, in case of $\alpha = 0$ purely resistive. The Warburg impedance describes the impedance of mass transfer. It depends on the transport of reactants through the electrolyte solution and is prominent at low frequencies, when diffusion dominates the sequence of electrochemical processes. In circuit representation,

reactions that occur consequently are represented by a series connection of elements. If processes occur simultaneously, their associated electrical equivalents are placed in parallel [131,133,134].

Table 2-3: Overview on the most relevant components in electrical equivalent circuit fitting. ω is the angular frequency, Y_0 the capacitance, α the exponent describing the capacitive/resistive properties of the CPE [134].

Component	Symbol	Impedance representation
Resistor	R	$Z = R$
Capacitor	C	$Z = \frac{1}{i\omega C}$
Constant Phase Element (CPE)	Q	$Z = \frac{1}{Y_0(i\omega)^\alpha}$
Inductor	L	$Z = i\omega L$
Warburg impedance	W	$Z = \frac{1}{Y_0\sqrt{i\omega}}$

Figure 2.49 shows an electrical equivalent circuit that is used to fit an electrode immersed into an electrolyte solution, also referred to as Randles circuit. At the interface, a double layer, made up of several individual layers is formed. The innermost layer, the inner Helmholtz plane (IHP), is made up of specifically adsorbed solvent and adsorbents. Solvated ions can approach the electrode only up to a larger distance, bound by the so-called outer Helmholtz plane (OHP). The presence of non-specifically adsorbed ions stretches out into a diffusion layer, extending from the OHP to the bulk electrolyte solution. The currents resulting from charging the double layer capacitor formed at the interface are mirrored in C_d. The charge transfer resistance (depicted as R_p) represents the resistance towards an electron transfer across the electrode/electrolyte-interface. This is a fast occurring process; hence, the kinetic control of this process is mirrored in the higher frequency domain. For this charge transfer to occur, reactants need to be transported to the interface. This is a diffusion controlled process, dominant in the low frequency region. The Warburg impedance Z_w represents this frequency-dependent resistive component. R_s represents the overall solution resistance. The modelling of a system according to the Randles circuit allows an evaluation of the environment that the sample electrode is placed in at its reaction towards this environment. A fitting of the electrical equivalents can give extensive information on resistive and capacitive properties of the system and accordingly evaluate the rate-determining steps of a reaction [135,136].

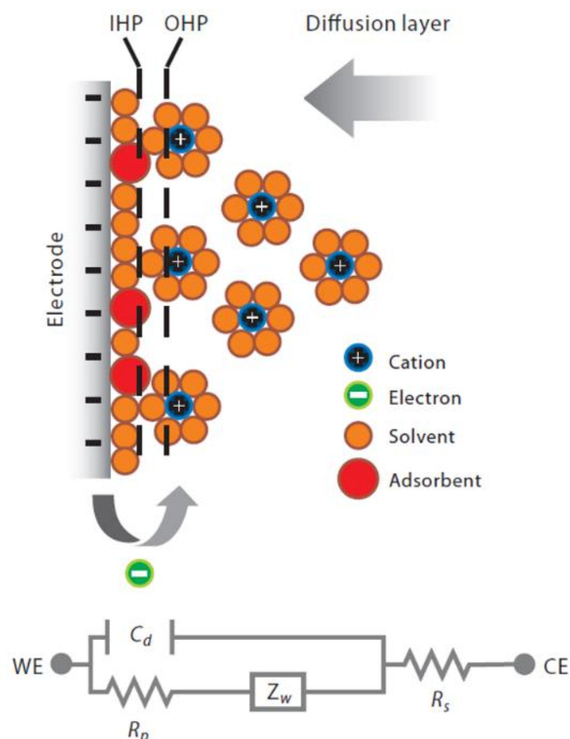


Figure 2.49: Electrode immersed into an electrolyte solution and formation of double layer with inner Helmholtz plane (IHP) and outer Helmholtz plane (OHP) along with electrical equivalent circuit [136].

A listing of a variety of electrical equivalent circuits along with accompanying Nyquist and Bode plots is depicted in Figure 2.50. The circuits cover a wide range of various frequency dependencies [133]. The biggest challenge in fitting measurement data to an electrical equivalent circuit is the general ambiguity of the data. Assigning a correct circuit does not only require formal fitting of the experimental results. It also requires a general understanding of the physicochemical system that is under investigation. Misinterpretation of measurement data leads to incorrect assessment of the sample in its surrounding. However, once an adequate model is found for experimental data, it can be used to determine different parameters of a system, like resistances or capacitances. This way, a model understanding of potentially occurring processes can be obtained [131,137].

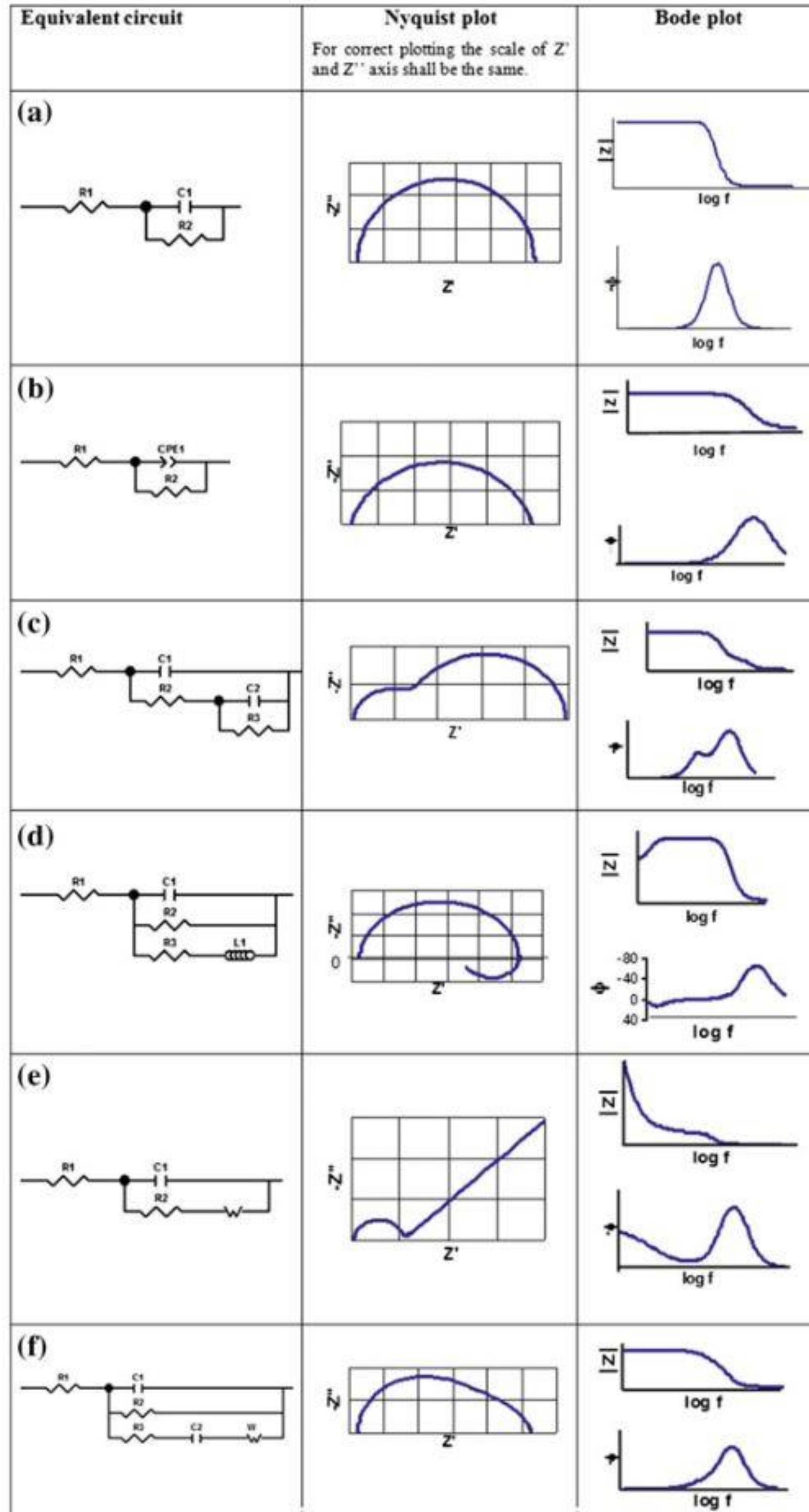
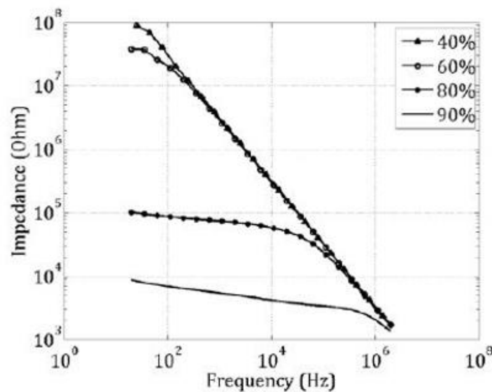


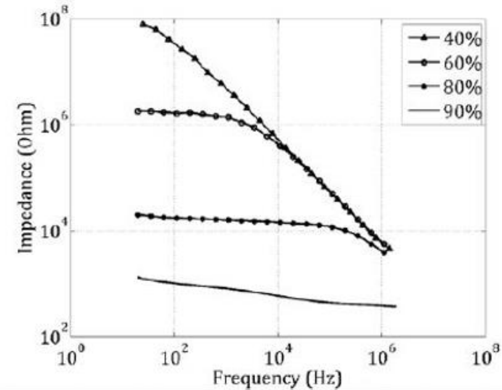
Figure 2.50: Electrical equivalent circuits with accompanying Nyquist and Bode plot representation [133].

Various studies demonstrate EIS' capability to assess climatic reliability of electronics. Other than the described extensive information that the technique provides about a sample, especially the non-destructiveness to the sample is of great advantage. The fact that EIS is able to distinguish between dielectric and electric properties allows broad investigations particularly with regard to humidity robustness. Consequently, key variables like specific resistance or permittivity changes can be easily assessed by EIS. Thus, it comes to use for instance in retracing the water uptake of epoxy-coated alloys [138]. In addition, the effect of dust on PCBA reliability under different relative humidity conditions can be analyzed by impedance spectra. Contamination results in enhanced water adsorption to the surface with increasing ambient humidity. This is represented by an impedance decrease. The EIS measurements also revealed that indoor dust samples are more sensitive towards changes in ambient humidity than outdoor dust samples (Figure 2.51a) and b)) [139]. EIS has also proven to be useful when evaluating the impact of solder flux residues on humidity interaction with PCBs based on their deliquescence behavior [83,140]. Figure 2.51c) shows an exemplary Bode plot of a Cu-Ni-Au electrode on an FR-4-board with succinic acid contamination. Increasing humidity levels are represented in the impedance drop across the whole frequency spectrum and a phase shift towards less negative values in the high frequency range [105]. With regard to corrosion just around the dew point and thin electrolyte layer formation, EIS was also demonstrated to estimate corrosion behavior by equivalent circuit fitting of measurement data [141]. EIS is also used for subsequent analysis of electronics in order to study the occurrence of corrosion products after climatic testing or in between exposure cycles. This way, for example, copper corrosion can be comprehended and corrosion products can be evaluated in terms of their possible protective function on the metal. Also, the corrosion rates of solders or other metal compounds like steel can be estimated by interpretation of EIS parameters [142–145].

(a) Bode Plot for outdoor dust



(b) Bode plot for indoor dust



(c) Bode plot for succinic acid

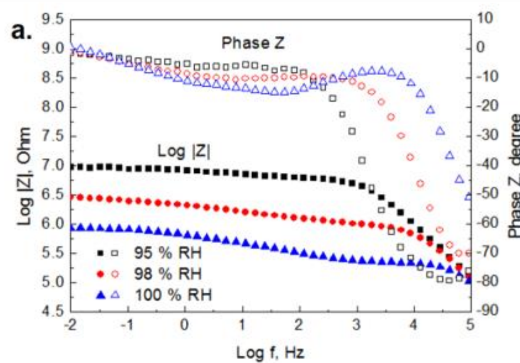


Figure 2.51: Bode plots of test patterns contaminated with outdoor dust (a) indoor dust (b) and succinic acid (c) under different humidity levels, adapted from [105,139].

2.4.3 Comparison of EIS and DC measurement techniques

In a comparative examination of EIS and DC measurement with regard to assessing climatic reliability of electronics, EIS has some benefits. Especially when wanting to assess ECM-related failure causes, the advantages are prominent. Underlying cause for ECM is the presence of a thin water layer between metal contacts. Understanding the formation of such a water film, possibly with dissolved contaminants is therefore considered crucial for precise reliability evaluation. SIR and EIS however, have different capabilities of detecting such a water film buildup (Figure 2.52). The electrical equivalent for an SIR test of the given scenario shows that the method is only able to detect an elementary conduction, determined either by conductivity of the space in between the comb patterns (R_C) or the transition of electronic conduction to ionic conduction at the electrode/electrolyte interface (R_{ct}, Z_W). EIS however, can give a more holistic picture due to its AC signal application. Also capacitive circuit elements (C_C describing the capacitance of the comb pattern and C_{dl} the double layer capacity) can be taken into consideration. The possibility to distinguish between these parameters as well as considering them in combination enables a

more detailed understanding of the test pattern in its surrounding from the EIS data. The SIR measurement is not able to distinguish individual processes and accordingly not suitable to gradual water film buildup as initial requirement for ECM [8,131].

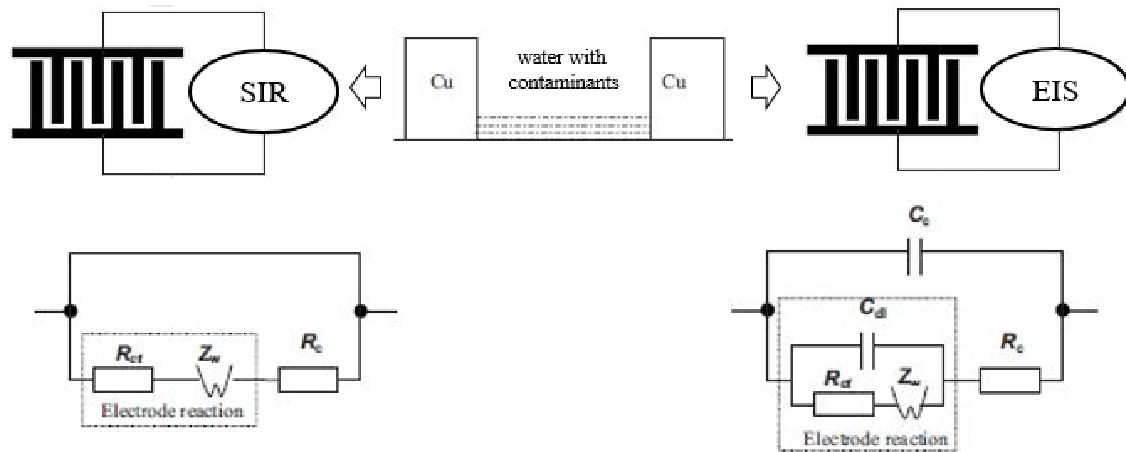


Figure 2.52: Electrical equivalent circuits for an SIR and an EIS measurement of copper comb patterns with a thin electrolyte layer in the gap, adapted from [8].

EIS' capability of detecting different conduction mechanisms by using a broad frequency band might also enable precise information on presence, amount and location of ionic contaminants. The possibility of measuring at all PCBA spots that can be electrically connected can be used to overcome ROSE and IC analysis' problems of overlooking residues below low stand-off components or contamination only localized at critical areas but present only in small amounts when considering a whole board [127]. Despite the mentioned benefits of the technique as well as the non-destructiveness to the sample, EIS is not yet used in standardized manner during development of PCBA setups. Alternative methods like SIR are considered less complicated and have the advantage of a history of standardization work. For the EIS measurement to be potentially used in the future, it is moreover necessary, to establish a link between the EIS data and the dendrite failure, which need the DC application to occur. The establishment of a correlation of ECM-critical EIS values can then again be used for a non-destructive holistic approach on PCBA climatic reliability assessment.

3. SUMMARY OF THE PROJECT AND LITERATURE REVIEW

This chapter provides a brief overview on the work carried out during the thesis project against the background of the state of the art knowledge, summarized in the literature review.

The manufacturing of automotive electronics involves various process steps and the combination of a variety of different materials (Chapter 2.1). Humidity induced failure mechanisms are a common problem of the complex setups. The detrimental effects are manifold, ranging from malfunction caused by humidity absorption, like CAF or change in dielectric properties, as mentioned in Chapter 2.3.1, to damaging processes on the PCB surface. Especially relevant in this context are SIR reduction or ECM (Chapter 2.3.2). In order to prevent the occurrence of the mentioned mechanisms, particularly the formation of a thin water film on the PCBA surface as precondition for corrosion is important to understand. In Chapter 2.2.2 it was shown that a number of studies has been performed with the focus on condensation events on different surfaces. Growth of isolated droplets as well as merging behavior that establishes surface water on an extended geometrical scale has so far been evaluated primarily by optical means. The impact of surface morphology or surface contaminants on the condensation process is therefore known. Likewise, there are many techniques available that can be used for humidity detection per se, described in Chapter 2.2.3. These range from mechanical sensors, capacitive or resistive methods to optical absorption approaches, becoming arbitrarily complex. Even though a number of sensory systems are available, their applicability in relation to PCBA electronics reliability is restricted. Sole knowledge on humidity estimates on a surface or its ambient are not transferable to corrosion failures. This is why in the context of PCBA climatic reliability, the issue of humidity related failure modes is commonly assessed by DC testing like SIR (Chapter 2.4.1). The leakage current that is detected for different temperature and humidity surroundings of a test PCBA allows drawing of conclusions on whether dendrite growth resulting from ECM has occurred. Accordingly, materials and designs are tested for their corrosion durability. The DC approaches however do not detect in detail the local humidity of water load per se. This is a frequently mentioned problem in literature, as it impedes a cause-effect relationship after failure occurrence in many cases and pseudo-failures or inexplicable test failures are common issues. EIS is therefore presented in this work as alternative method that allows detection of successive changes in condensation and water bridge buildup, leading up to electrical breakdown. As explained in Chapter 2.4.2, EIS is conventionally used in electrochemistry in order to model conduction processes for systems of electrodes immersed in electrolytes. However, some investigations have also shown for EIS to be able to distinguish thin electrolyte layer properties. This indicates promising results for using EIS to retrace the stepwise water film buildup from the earliest stages of condensation until formation of an interconnecting film between test electrodes on a PCB.

However, no detailed investigations looking into the use of EIS parameters to assess a dendrite failure have been established yet (Chapter 2.4.3). The aim of this work is to bridge this gap and provide a basis for evaluating EIS as possible alternative method for PCBA humidity robustness valuation. In order to do so, different aspects that have not yet been the subject of detailed literature have been conducted. This includes an initial validation of the capability of EIS to detect water film buildup on a PCB in general and relate it with intermittent DC measurement to establish threshold values when using EIS for ECM-risk assessment, as presented in Chapter 6 and Chapter 7. The possibility of non-DC methods to detect localized condensation due to PCBA factors like temperature distribution or contaminants is further evaluated in Chapter 8. Chapter 9 provides an all-embracing review on using EIS as prediction of PCBA failures related to different climatic affects, as well as surface and design impacts. The holistic understanding of humidity induced failures mechanisms in electronics is one of the key aspects in robustness evaluation of PCBAs. With the work carried out, an impact can be made in the field of electronics reliability. EIS can be used to characterize conductive processes on the PCBA without causing irreversible reactions as during DC measurements and allow the screening of a system under different humidity conditions in much shorter time, with fewer samples and higher confidence level. Consequently, the translation of EIS data on water film formation and respectively occurring electrochemical processes can also be used to develop design guidelines for PCBA setups.

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4. MATERIALS AND METHODS

4.1. TEST BOARDS

4.1.1 SIR test patterns on FR-4 laminate with and without solder mask

The studies were primarily conducted on cleaned FR-4 laminate glass fiber reinforced epoxy resin test boards. The thickness of the laminate was approximately 1.6 mm. The measurement structures were standardized SIR comb patterns with interdigital electrode arrangement with copper surface. If a surface finish was used it was Organic Solderability Preservative (OSP). The Cu-width in the area of the comb patterns was 200 µm. Patterns had different gap sizes namely 100 µm, 200 µm, 300 µm and 600 µm (Figure 4.1a)). These distances match with the common gap sizes on PCBAs for automotive applications. The typical morphology of the laminate is shown in the SEM image in Figure 4.1b). Some experiments were done on the comb patterns with solder mask as base layer (Figure 4.1c)). Prior to testing, all boards were cleaned in a bath consisting of 75 % Isopropyl alcohol and 25 % DI-water, kept at 45 °C (based on IPC-TM-650, Method 2.3.25) for 20 minutes. For subsequent drying, they were stored in a desiccator filled with silica gel for a duration of at least twelve hours.

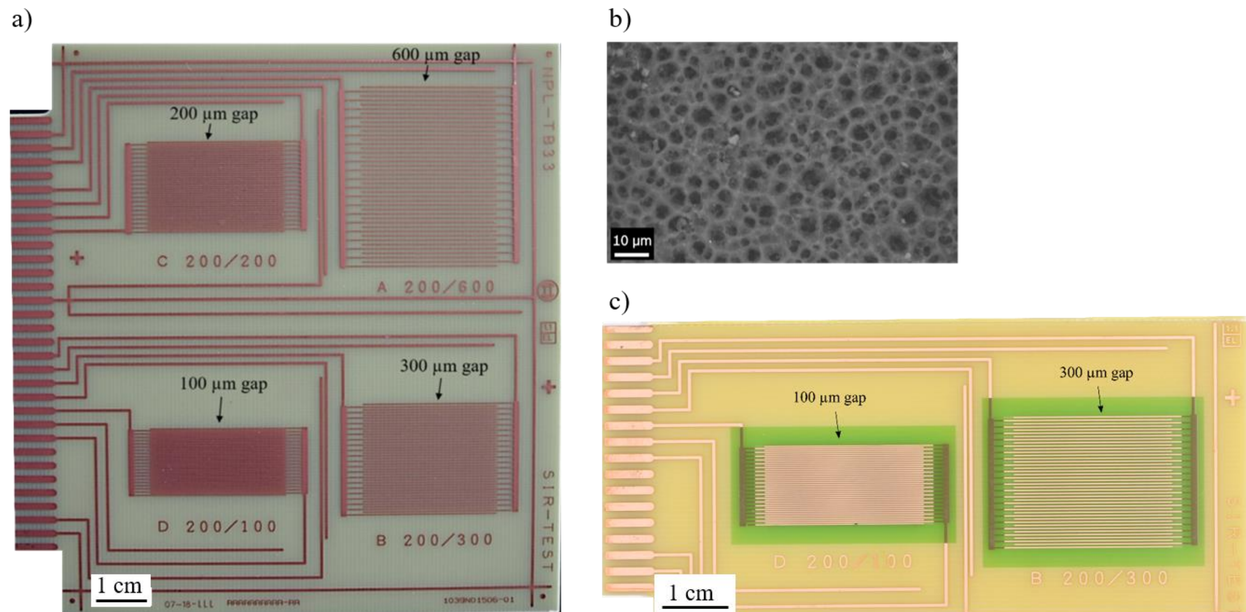

Figure 4.1: a) Photograph of a typical test SIR comb pattern specimen used for testing. Gap sizes are indicated in the picture. b) Exemplary SEM image of the FR-4 surface laminate between the Cu-gaps. c) Photograph of a typical SIR comb pattern specimen with solder mask surface in the region of the 100 µm and 300 µm interdigital regions.

4.1.2 Tin T-shaped test patterns on FR-4 laminate

In order to establish a clear correlation of electrochemical processes taking place on the electrodes with full view camera recording of water film buildup, test patterns with a narrow opposing anode-cathode area were used (600 µm). In addition, the samples served a more accurate classification of EIS-signal and growth of a gap bridging dendrite. The substrate material was standard FR-4 laminate with 1.6 mm thickness with two opposing T-shaped tin-structures functioned as electrodes (Figure 4.2). The Sn-width was 200 µm. The gap size was 125 µm.

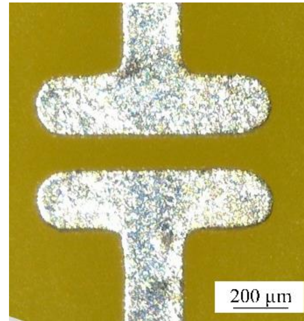

Figure 4.2: Tin pattern with narrow opposing anode-cathode region with 125 µm gap on FR-4 laminate.

4.1.3 SIR test patterns on LTCC

Measurements were conducted also on comb test patterns on LTCC (Low Temperature Cofired Ceramic, Glass-Al_2O_3-Ceramic) surface using AgNiPdAu as metallization. The overall area of the comb patterns was smaller and with less interdigitated arms compared to the patterns on FR-4 surface. However, the track width was also 200 µm. Similar to FR-4 based test objects, the combs with a gap size of 300 µm were used (Figure 4.3a)). Compared to the FR-4 laminate, the LTCC has a smoother surface morphology (Figure 4.3b)).

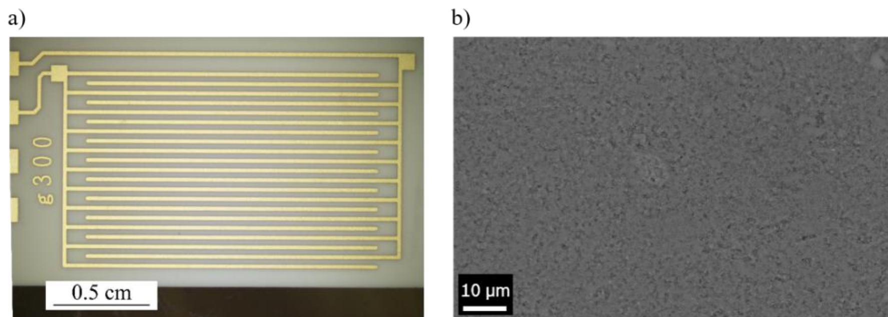

Figure 4.3: a) Photograph of a 300 µm gap comb pattern on LTCC surface. b) Exemplary SEM image of the LTCC surface.

4.1.4 FR-4 laminate with assembled BGAs

Assembly level testing with components was performed on boards with assembled Ball Grid components. Electrochemical Impedance Spectroscopy and intermittent DC leakage current measurements were performed on the circuitry below the SMT-soldered BGAs. One measurement channel contacted two BGAs (Figure 4.4). The substrate of the boards was standard FR-4, covered with solder mask, however not in the component region. Below the components, surface was solely comprised of an interdigitated tin pattern, with eight tracks each, connecting the 16 x 16 solder pads. The solder used for assembly was a standard automotive SnAgCu based SMD no-clean solder paste. The solder balls had a pitch distance of 300 µm. The standoff of the components after reflow soldering was approx. 150 µm. No additional cleaning step took place after manufacturing in order to create series-manufactured ECU conditions.

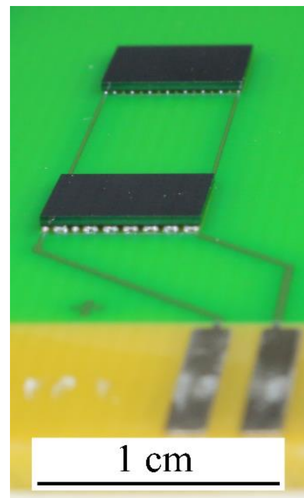

Figure 4.4: Test pattern of two BGAs each soldered onto a comb pattern layout on a standard FR-4 board.

4.1.5 Time Domain Reflectometry patterns

To perform Time Domain Reflectometry (TDR) measurements, two different kinds of test patterns were used. Both were based on two parallel Cu-traces for differential pair measurements. The tracks were inner layers, covered with soldermask. Electrical connection was achieved via soldered SMA connectors. Both samples differed in length of the parallel traces, namely for one pattern it was 90 mm (Figure 4.5) and for the other pattern 120 mm.

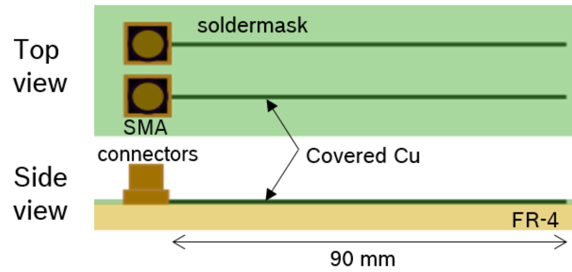

Figure 4.5: Schematic representation of top view and side view of a TDR pattern comprised of two parallel Cu tracks of 90 mm length. Covered with solder mask and soldered SMA connectors.

4.1.6 Flux Contamination

To investigate the relationship between condensation processes and flux residues on a PCBA surface, a commercially selective flux in standard automotive version was used. It was a Low-VOC (volatile organic compound) resin based general wave solder flux, which was designed for a no-clean process. In a not fully cured state, it was dispensed on test patterns to study dewing in the residue region.

4.1.7 PCB with comb pattern matrix

In order to use AC impedance measurements to generate a humidity map across a larger PCB surface area under temperature and humidity conditions, a comb pattern matrix sample The test patterns were interdigital Cu comb patterns with each 200 µm track width and 100 µm gap. One comb pattern was 3 mm x 3 mm in dimension. Distance between the individual patterns was 0.7 mm (Figure 4.6). In total, a matrix of 7 x 8 patterns was measured. Substrate material was standard FR-4 laminate without solder mask in the area of the comb patterns. The goal was also to generate an inhomogeneous temperature distribution across the test pattern, recreating the field case of heat-generating powered components. In order to create a local heat source, the test board had a SMT diode mounted in the middle two comb patterns of the matrix by means of a heat conducting paste. The diode was powered with an external power supply during testing with either 0.2 A or 0.4 A to evaluate the heating impact.

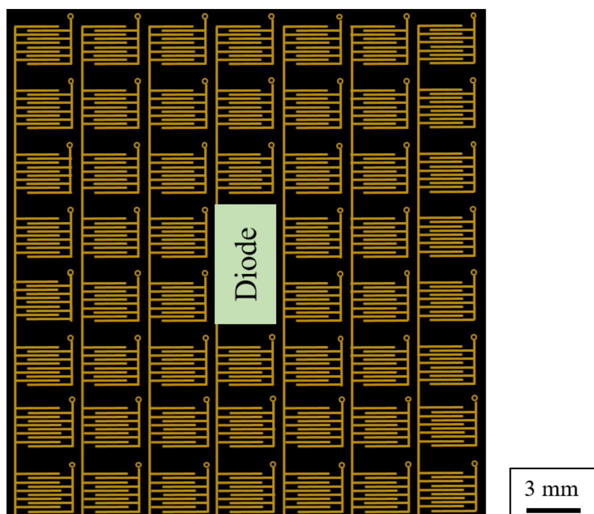

Figure 4.6: Schematic representation of 7 x 8 comb pattern matrix with SMT diode placed onto the middle two comb patterns.

4.2. CLIMATIC TESTING

4.2.1 Climatic Chambers

Climatic tests were performed primarily in an "Espec PL-3 J" climatic chamber (ESPEC Corp., Japan), providing a global temperature range between −40 °C and 150 °C, and ambient relative humidity (RH) between 20 % and 98 %. For short-time combined EIS and DC testing on LTCC samples and T-shaped patterns on FR-4 laminate, as well as Time Domain Reflectometry measurements, a benchtop temperature and humidity chamber was used (SH-242, ESPEC Corp., Japan). AC impedance experiments to assess the condensation impact of a heat-radiating diode were conducted in a "VCL4010" environmental test chamber (Vötsch, Germany).

4.2.2 Peltier Cooling Stage

Experiments that were supposed to provoke gradual condensation on the test patterns, the samples were actively cooled with a Peltier Cooling Stage (CP-031, TE Technology Inc., USA). Patterns were mounted on top of the cooling stage by means of a Non-Silicone Heat Transfer Compound (Electrolube, UK). The Peltier stage itself was powered by a DC power supply. To ensure dissipation of generated heat during testing, the stage was equipped with a bottom side fan. A Heat & Cool Bipolar controller (TC-720 OEM, TE Technology Inc., USA) in combination with thermocouples sensors (MP-3139, TE Technology Inc. USA) mounted on the test boards, allowed regulation of the cooling profile.

4.2.3 In-situ camera recordings

To trace the water film buildup or dendrite growth, some of the experiments were monitored in-situ with a USB Microscope Camera (AM4115ZTL, Dino-Lite). A tripod was used to fix the camera in the climatic chamber above the samples. External controlling of the camera via a USB-connection to the measurement laptop enabled situational adjustment of the LED-illumination and taking of images or videos during testing.

4.3. ELECTRICAL/ELECTROCHEMICAL CHARACTERIZATION

4.3.1 Potentiostat

Electrochemical Impedance Spectroscopy (EIS) and DC leakage current measurements in combined intermittent or in separate mode were performed with an electrochemical workstation (VMP3, BioLogic Science Instruments, France). The setup enabled both measurement modes alternatingly on the same channel. Testing was performed using a two electrode setup. DC potentials between 1.667 V and 10 V were used. EIS was done in the frequency ranges between 100 mHz and 100 kHz. AC voltages were in the range of 5 mV – 10 mV

4.3.2 Electrical Equivalent Circuit Fitting

Fitting EIS data to electrical equivalent circuits was performed by means of *EC-Lab®* software (V11.20, BioLogic Science Instruments). Alternatively, the software *ZSimpWin* was used.

4.3.3 Time Domain Reflectometry

The experiments involving Time Domain Reflectometry (TDR) were performed with Controlled Impedance Test System (CITS 880s, Polar Instruments). The differential mode of the technique was employed, meaning a signal with an amplitude of 300 mV and rise time ≤ 200 ps was sent through two parallel measurement lines. Adjustment of specimen spatial length and impedance data curve was conducted by means of the manufacturer’s accompanying software.

4.3.4 AC impedance matrix measurements

Condensation tests on the comb patterns in matrix circuitry were performed with an in-house built potentiostat system. It provided a signal amplitude of 3 V at a frequency of 10 kHz. The impedance for all of the regarded single comb patterns was measured over time. The successive value obtainment in matrix mode leads to recording of a pattern value every 13 seconds.

4.4. OTHER MATERIAL CHARACTERIZATION TECHNIQUES

4.4.1 Optical Microscopy, cross-sectioning and SEM/EDX

Images of samples as well as embedded specimen from cross sectioning were obtained with Olympus BX51M, Olympus SZX16 or Keyence VHX-600D. Cross sections were prepared with TegraPol-31, TegraPol-32 or Tegramin-30 by Struers. A qualitative analysis of the surface morphology in the microscale was carried out with an SEM EVO60 (Zeiss).

4.4.2 Contact angle measurements

Evaluation of wetting properties for different substrate materials was performed by static contact angle measurements with a Drop Shape Analyzer (DSA25, Krüss GbmH). The contact angle of 5 µl Millipore water droplets set on the surface was given by the angle between shape line of droplet curvature and the sample surface.

5. SUMMARY OF APPENDED PAPERS

5.1. COMBINED EIS AND DC LEAKAGE CURRENT MEASUREMENTS TO EVALUATE THE PROCESS OF WATER FILM FORMATION AND SUBSEQUENT DENDRITE GROWTH ON ELECTRONIC ASSEMBLIES

Objectives:

- Investigate the process of water film formation between interdigital copper comb patterns of different gap sizes on a PCB surface.
- Use EIS measurement and in-situ optical microscopy during active cooling of samples below dew point to track the condensation.
- Correlate the EIS information on water film buildup with the leakage current development based on parallel DC measurements to assess ECM-critical EIS values that predict dendrite formation upon DC bias application.

Findings:

- ➢ EIS measurements display the formation of a water film by a drop in impedance and a shift in phase angle towards zero value. The gradual change in the impedance at a frequency is valid for all frequencies from 1 kHz to 100 kHz (Figure 5.1). The higher frequency range shows the largest value delta from dry to wet status.
- ➢ In DC measurements, two different current regimes were distinguishable during condensation and related to ECM. For currents between 1 x 10^{-4} mA – 1 x 10^{-2} mA, condensate islands are microscopically visible and at the end of the range ECM is possible. Dendrites bridging the electrode gap are indicated by the current exceeding 1 x 10^{-2} mA. The temporal reaching of both regimes depends on the electrode distance; smaller gap sizes are bridged earlier and develop ECM first.
- ➢ By comparing EIS and DC Leakage Current tests, it can be stated that the reduction of EIS impedance at 45 kHz below 50 % of dry board value signifies dew formation pronounced enough to enable ECM in case of a 5 V DC application.

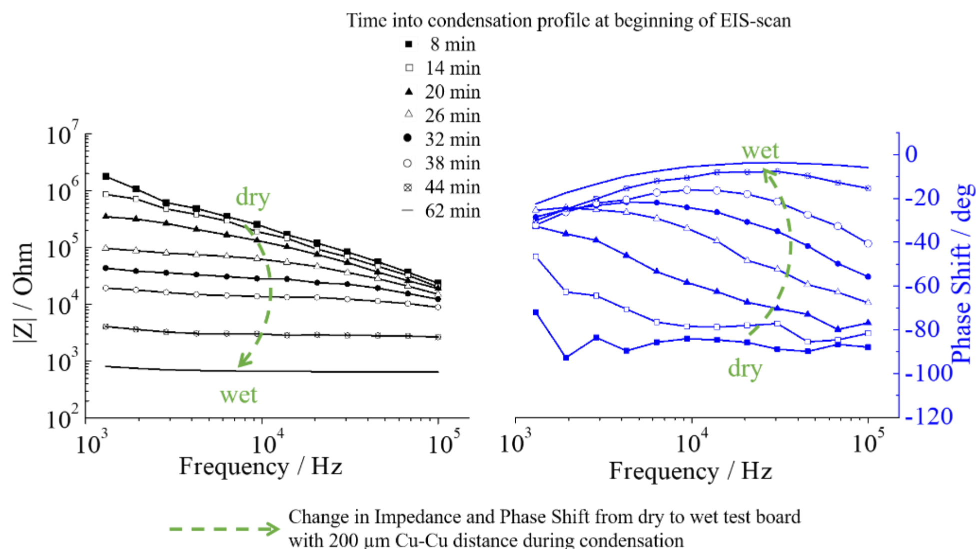

Figure 5.1: EIS scans during progressive water film buildup (dry → wet) for a 200 µm gap copper comb structure.

5.2. COMBINED APPROACH OF EIS WITH INTERMITTENT DC TO EVALUATE THE ECM RISK OF PCB TEST BOARDS UNDER CONDENSING CONDITIONS

Objectives:

- Understand the condensation mechanism on different PCB surfaces and establish alternating measurement modes of EIS and DC to trace the water film buildup by means of EIS and determine a potential dendrite criticality by intermittent DC application.
- Perform gravimetric water amount measurements during climatic testing to assess the water layer thickness in different condensation regimes.
- Investigate change in EIS values prior to DC dendrite formation to evaluate EIS as non-destructive predictive tool for ECM.

Findings:

- Data obtained from alternating EIS and DC shows pronounced changes in EIS' resistive and capacitive parameters prior to DC failure. This allows the assignment of EIS values signifying a water layer pronounced enough to enable ECM. An impedance decrease to approx. 2 x 10^4 Ohm for 68 kHz frequency was shown to be ECM critical for all of the tested samples (Figure 5.2, Type A-D, "dendrites" regime) independent of surface material or Cu-Cu distance.
- Gravimetric measurements during condensation testing showed that the average amount of water on the specimen doubles from the point to first detection of condensation in DC measurements until the formation of closed dendrites. The water layer thickness in the dendrite growth range can be associated with "bulk water" layer thickness. EIS measurements can identify the transition of water layer buildup into this range.

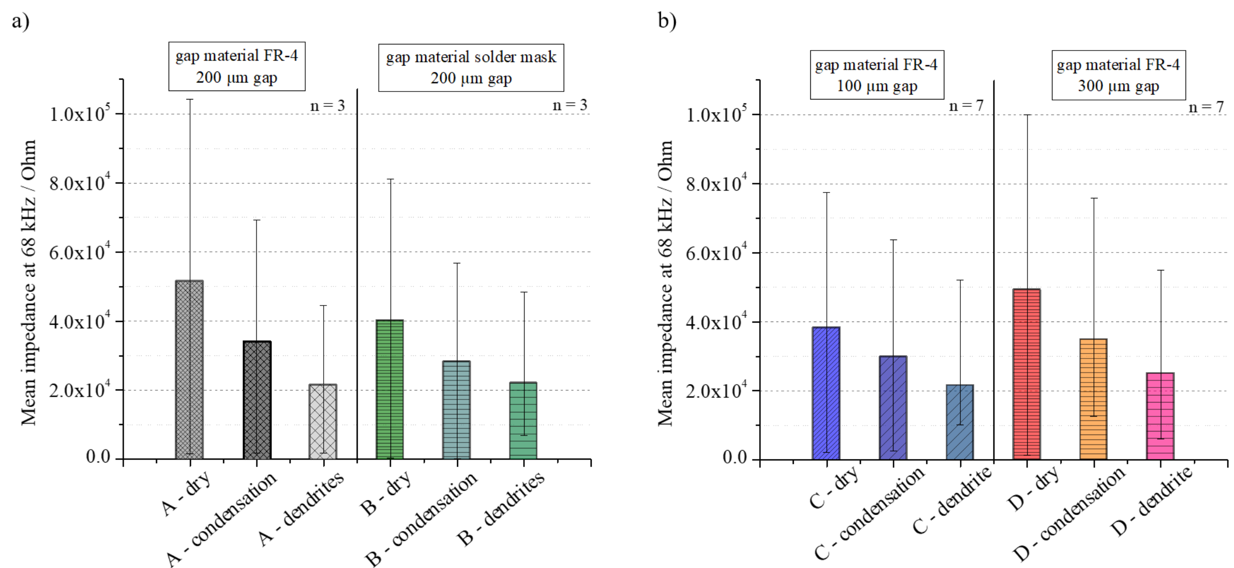

Figure 5.2: Mean impedance at 68 kHz indicating "dry" board status, as well as the progression into "condensation" and "dendrites" water layer regime for a) 200 µm gap samples on FR-4 and solder mask surface and b) 100 µm and 300 µm gap samples on FR-4.

5.3. NON-DESTRUCTIVE ELECTRICAL APPROACHES TO LOCALIZE CONDENSATION EVENTS ON PCBS

Objectives:

- Determine localized condensation events on PCB surfaces by the use of impedance and TDR measurements
- Use AC impedance to create a humidity map profile of a PCB surface with a matrix of interdigitated comb patterns around a heat-generating diode component in different climatic scenarios. Employ the impedance data of the comb patterns to assess non-homogeneous condensation in the diode surrounding and establish ECM-safe areas close to the heating component.
- Use TDR measurements to locate water droplets of different volumes located at different locations on a solder mask covered copper traces. Apply TDR to detect the different condensation severity at spots with and without flux residues on a PCB surface.

Findings:

- Impedance values of a comb pattern matrix are able to display different levels of non-homogeneous condensation around heat-radiating diode (Figure 5.3). By relating the impedance values to the establishment of an electrode-bridging water film, ECM-safe areas around the diode component can be calculated for distinct climatic scenarios. This testing approach can be used for optimized placement of heat-radiating components during PCBA design to improve humidity robustness.
- TDR measurements can be used to distinguish water droplet volume by a reduction in impedance. Likewise, the spatial resolution of the measurement allowed to localize the droplets placed along the length of Cu-traces. It can also be employed to detect repeated condensation and evaporation processes on a PCB surfaces. By relating impedance to pattern length, it is also possible to detect locally enhanced condensation at spots with flux residue.

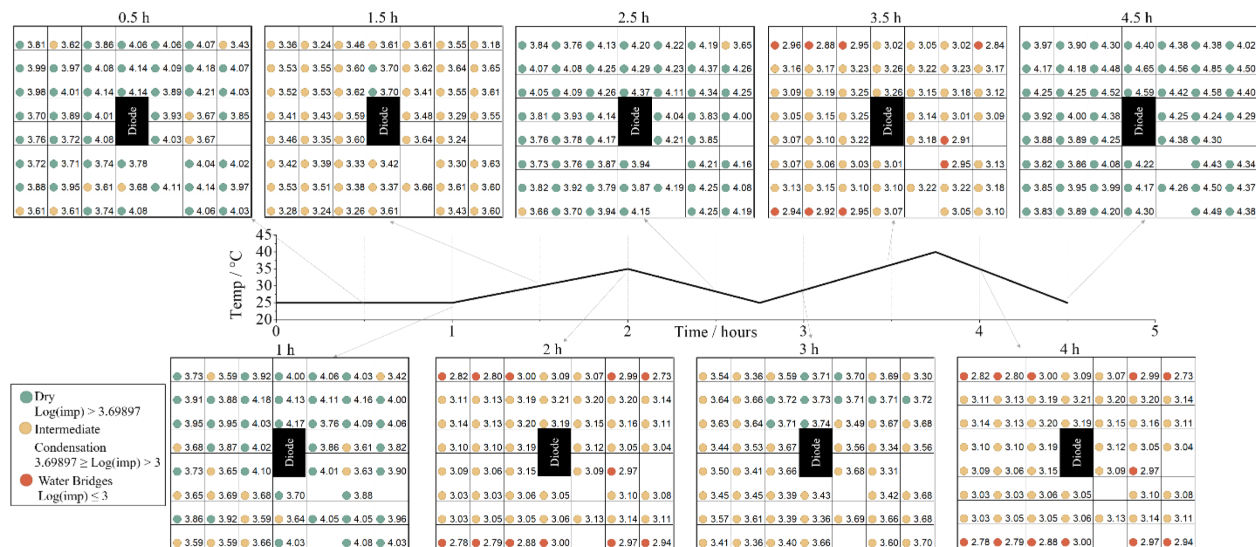

Figure 5.3: Classification of "dry", "intermediate condensation" and "water bridges" state based on impedance values of test patterns around a heat-generating diode during a cyclic climatic profile.

5.4. ON THE FEASIBILITY OF ELECTROCHEMICAL IMPEDANCE SPECTROSCOPY TO ASSESSS CLIMATIC RELIABILITY OF PRINTED CIRCUIT BOARD ASSEMBLIES

Objectives:

- Summarize information on the feasibility of EIS as a test method for humidity induced failures on electronics.
- Provide an overview of studies and complementary work with regard to using EIS as a method to assess electrochemical migration for different types of test pattern geometries and substrate materials.
- Display the benefits of EIS for early detection of critical humidity states on PCBA setups with assembled components.
- Assess the advantages and drawbacks of using the EIS approach instead of the conventional DC tests and evaluate the potential of EIS as a future test method for humidity-related reliability.

Findings:

- ➢ EIS can be used as a non-destructive method to display the successive steps in water layer buildup on PCB and ceramic substrates.
- ➢ Changes in resistive and capacitive EIS parameters can be used for determination of an ECM-critical water film in case of DC application.
- ➢ On boards with soldered components, changes in EIS capacitive parameters display humidity states on the PCB surface that the DC testing is not able to replicate (Figure 5.4).
- ➢ The benefits of EIS as being non-destructive and delivering more comprehensive information on criticality make it a promising method for climatic reliability testing in the future.

a) Test board with soldered BGA components   b) Progression of DC Leakage Current and EIS capacitance during cyclic climatic profile

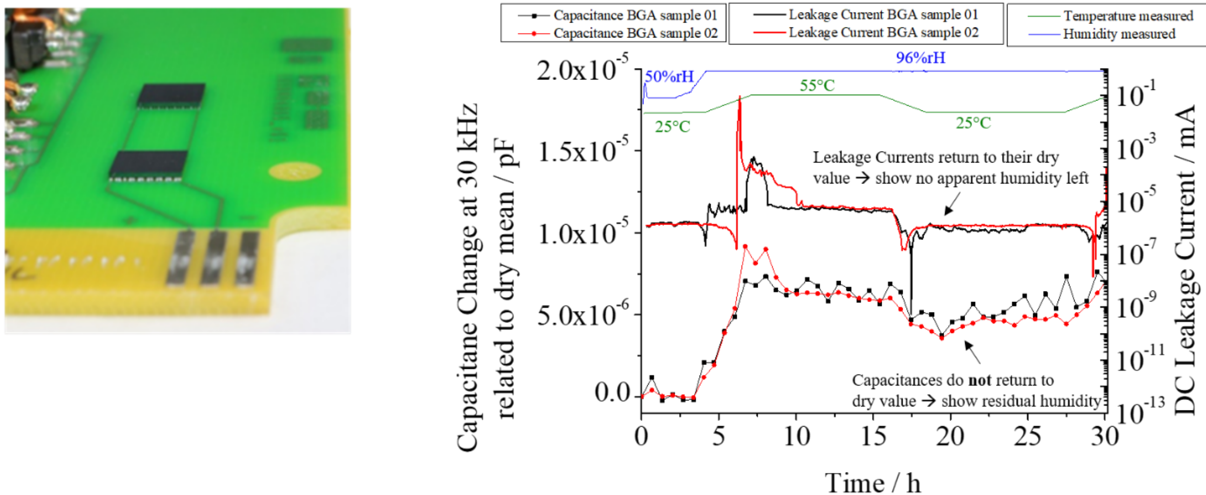

Figure 5.4: Photograph of test board with assembled BGAs (a) and signal progression of DC leakage current and EIS-capacitance over the course of cyclic temperature profile (25 °C-55 °C at 96 %rH).

6. COMBINED EIS AND DC LEAKAGE CURRENT MEASUREMENTS TO EVALUATE THE PROCESS OF WATER FILM FORMATION AND SUBSEQUENT DENDRITE GROWTH ON ELECTRONIC ASSEMBLIES

Simone Lauser, Theresia M. M. Richter, Vadimas Verdingovas, Rajan Ambat

Abstract – Investigations in this paper focus on understanding the water film buildup on Printed Circuit Board Assemblies (PCBA) under humid condition and subsequent electrochemical processes leading to failures by use of combined Electrochemical Impedance Spectroscopy (EIS) and DC voltage measurements. The FR-4-substrate used contained interdigitated copper electrodes with different distances, which were exposed to condensing conditions by cooling below dew point in a controlled ambient climate. An AC excitation voltage of 10 mV (frequency range between 1.3 kHz and 100 kHz) was used to detect the water bridge buildup during condensation. In parallel, the leakage current was monitored under DC potential (5 V bias) under varying water bridge conditions. The results show that the formation of dew up to the establishment of a condensate bridge can be identified by EIS. For 45 kHz it was found that an AC impedance of 2.4 x 10^4 Ohm (200 µm Cu-Cu distance), respectively 2.7 x 10^4 Ohm (300 µm Cu-Cu distance) describes the water film status that enables the formation of gap bridging dendrites upon a 5 V DC application. Based on this, EIS can be used non-destructively for risk evaluation of electrochemical migration on a PCBA surface.

Keywords – corrosion; electrochemical impedance spectroscopy; electronic reliability; humidity; surface insulation resistance; water film formation

I. INTRODUCTION

The trend towards miniaturization of electronics and their wide-spread use result in several humidity related reliability issues due to corrosive processes [1, 27]. The Printed Circuit Board Assembly (PCBA) as main component of electronic setups can be exposed to a variety of transient climatic conditions defined by humidity and temperature. The exposure can lead to the formation of thin water film depending on the humidity and temperature on the board surface [7, 25]. The electrical properties of the water film are essentially determined by the electrochemical aspects of the micro-cell formed on the PCBA surface. When a layer of dew and possibly dissolved contaminant connects neighboring biased points such as soldered connections or legs of components, corrosion failures are prone to occur. In many cases, these are not easy to identify during post-failure analysis because of the disappearance of the traces of water or fragmented dendrites formed due to electrochemical migration (ECM).

S. Lauser, T. M. M. Richter, V. Verdingovas and R. Ambat, "Combined EIS and DC Leakage Current measurements to evaluate the process of water film formation and subsequent dendrite growth on electronic assemblies", under revision in *IEEE Transactions on Device and Materials Reliability*, 2020.

ECM is one of the most prominent failure modes for electronics under humid conditions [2]. Easily reducible metals such as copper and tin on the PCBA cause ECM issues due to the dissolution of the metallic species at the anode, transport of these ions through the water film under electric field towards the cathode, and deposition in the form of a dendrite. Other parameters influencing the ECM are short distances between the electrodes, electric field due to applied potential bias, water film thickness, and chemistry of the film. Due to the formation of a dendrite, an electrical connection between anode and cathode can be established. This leads to a reduction of resistance between the biased points on the PCBA surface [2, 19]. ECM has been reported to occur for various metals such as for silver, copper, tin, and lead [10, 12, 23, 29]. However, the prior requirement for the ECM failure is the buildup of a substantial thickness of the water film, which leads to the development of faradaic reactions at the electrodes. Faradaic reactions at the oppositely biased and closely spaced electrodes cause the development of leakage current, which in itself can cause failure of electronics if it occurs on a PCBA and the current levels are higher than the affordable drift levels. Continuous occurrence of leak current can further lead to ECM failures due to metal dissolution, migration, and dendrite formation. However, the buildup of water film thickness to a distinct level is important because of the fact that progressive water film buildup results in reduced ohmic drop between electrodes. This sets conditions for faradaic reactions and increased current between anode and cathode.

The formation of thin electrolyte layers (TEL) on distinct surfaces in general is important for corrosion, therefore has been investigated in connection with various studies such design of cooling panels for air-conditioning systems [22] or for the performance of Magnesium based implants [30]. Former work focused on dew formation on a hydrophobic surface in comparison with untreated aluminum in order to understand the movement of droplets on the surface. The latter work focused on thicker water layers with thickness ranging from 50-500 µm. Due to the measurement setup, those layers however are considered uniform, meaning that it was not possible to state how the gradual buildup of an electrolyte layers determines corrosive processes. Other work took the approach to relate ECM in condensing conditions with the measured data of a capacitive microsensor, delivering information on the dewing [20]. Also, the dendrite growth kinetics under deionized water drops haven been investigated [8]. Hence, literature gives a general insight in dew formation on different surfaces, partially also in corrosion under thin layers, but it is still unclear, to what extent a water film needs to be established on electronics to enable the leak current failures and ECM.

To investigate the effect of dew formation on the surface of a PCBA, the commonly used test methods rely on the application of a DC voltage and the measurement of corresponding leakage currents. The leakage current develops at two levels: (i) due to the electrode reactions at anode and cathode and current flow between the electrodes through a solution layer, and (ii) higher current levels if the dendrite forms between

the electrodes. The so-called SIR (Surface Insulation Resistance) test underlies the fact that the measured resistance across the gap of two conducting materials is a property of the medium in between, hence detecting current leakage or electrical shorts. Thus, the method is regularly used to test electronic assembly materials and designs or process aspects such as the effect of solder flux on humidity related reliability issues under distinct climatic conditions [15, 16]. The general idea behind the test method is that under required applied DC potential bias, the faradaic current between the biased points exhibited as the leak current represents the level of parasitic circuit development over the PCBA that could interfere with the electronic functionality. Therefore, this method is widely used in understanding the humidity effects on electronics. It is not only a destructive test, but also it provides only little information of the water film characteristics due to polarization and local chemistry effects [6, 9, 21]. Correspondingly, the DC-based approach is not suitable to understand the progressive water film buildup under humid condition and the chain of events taking place due to the electrical property of the water film under biased conditions. Typical examples are the resistive and capacitive changes of the water film with thickness of the film, which will interfere with the functionality of the electrical circuits. When performing SIR tests, a typical DC bias of as high as 100 V is applied to the specimen under high humidity conditions [9]. While the electrical bias triggers the migration of ions due to the electric field, it also causes polarization on the surface of the electrodes. Hence, the gradual process of water film formation to build up a continuous path between anode and cathode is difficult from the DC methods for mechanistic understanding. On the other hand, for a majority of the cases, a DC voltage bias exists on a working PCBA, therefore understanding failure under DC bias condition is also equally important.

However, in order to study the gradual buildup of water film, AC techniques such as Electrochemical Impedance Spectroscopy (EIS) can be employed without having the drawbacks of the DC methods. An alternating voltage with a low amplitude is not only non-destructive to the sample, but can also be used for a detailed characterization of the electrical properties of the medium between two electrodes such as its capacitive and resistive character. Correspondingly, the process of condensation up to the point when a sufficient quantity of dew has formed to bridge the metal-metal gap can be detected. Due to the small perturbation voltage, EIS keeps the system essentially in equilibrium, meaning that the excitation is small enough not to evoke a non-linear response [18].

The goal of this work is to understand the process of condensation on the surface of PCBAs and to retrace the pathway of water film buildup and electrical interference mechanisms on a PCBA by means of EIS measurement with simultaneous DC measurements. In order to correlate the characteristics of water film formation to failure sequence, both AC and DC measurements were carried out on PCB substrates with two pairs of similar electrodes. These copper comb-structures with two pairs of Cu-Cu distances (200 µm and

300 µm) on FR-4 laminate were exposed to slowly condensing conditions. Electrochemical impedance under water film buildup was monitored in order to understand the change in the electrical characteristic of the water film, while the simultaneous DC measurement provided information on critical level of water loading at which substantial increase of leakage current occurs, leading to ECM possibility. Additionally, morphology of the water film build up was monitored in-situ using optical methods.

II. MATERIALS AND METHODS

A. Test Boards

The tests were carried out with interdigitated copper comb patterns with OSP (Organic Solderability Preservative)-finish on glass-fibre reinforced epoxy resin (FR-4) of 1.6 mm thickness. The size of the test PCBs was 62.5 mm x 125 mm. Two types of PCBs were used for the measurements namely: (i) shown in Figure 6.1 (left) with Cu-Cu distance of 200 µm and (ii) Figure 6.1 (right) with Cu-Cu distance of 300 µm. Other patterns on the PCBs shown in Figure 6.1 were not used for measurements. For both comb patterns, the width of the copper electrode was 200 µm. The use of the term “electrode” accordingly means 21 comb arms, whereby the height of the Cu is 30 µm and the lengths of the interdigitated area is 2.5 cm for both the 200 µm and 300 µm distances. These Cu-Cu distances selected for measurements in general match with the typical distances on a PCBA.

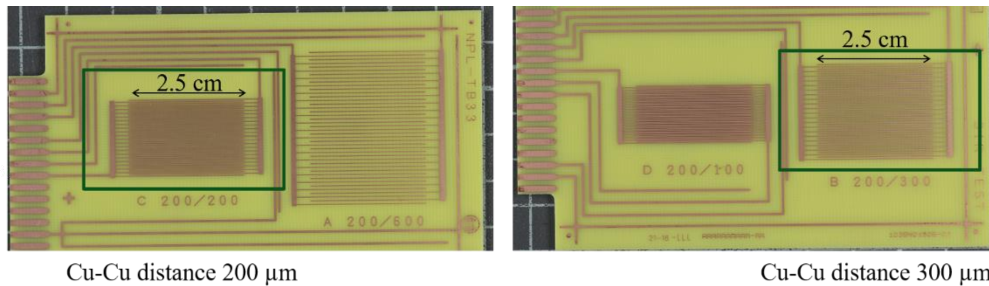

Figure 6.1: FR-4 test boards with copper comb structures of 200 µm width and gap sizes of 200 µm (left) and 300 µm (right) used for testing marked in green.

Prior to the condensation testing, the boards were cleaned in a bath consisting of 75 % Isopropyl alcohol and 25 % DI-water kept at 45 °C (based on IPC-TM-650, Method 2.3.25) for 20 minutes. Afterwards, the samples were rest to dry in a desiccator filled with silica gel for a duration of at least twelve hours.

B. Climatic chamber to provide constant testing environment

All tests were performed in an "Espec PL-3 J" climatic chamber (ESPEC Corp., Japan), providing a temperature range between −40 °C and 150 °C, and relative humidity (RH) between 20 % and 98 %. The chamber was set to provide a constant temperature and humidity environment of 25 °C and 92 %RH for creating local condensation experiments on PCBs shown in Figure 6.1 using a Peltier Cooling Stage.

C. Peltier Cooling Stage to provoke condensing conditions

The gradual buildup of water film on the test PCB surface has been achieved by the use of a Peltier Cooling Stage (CP-031, TE Technology Inc., USA). The contact cooling plate on the top of the Peltier elements allows direct mounting of the test specimens onto the stage. Heat transfer between the contact cooling plate and PCB substrates was achieved using a Non-Silicone Heat Transfer Compound (Electrolube, UK). The stage was powered by a separate DC power supply and the Peltier stage had a fan at the bottom to remove the heat generated at the bottom side of the setup. Control of the Peltier stage for precise temperature was achieved using a Heat & Cool Bipolar Controller (TC-720 OEM, TE Technology Inc., USA), driven by a separate power supply. To provide the controlling unit with the respective current temperature status of the test boards, a thermocouple (MP-3139, TE Technology Inc. USA) was mounted on top of the test boards using the heat transfer compound and connected to the controller inputs. The controller regulated the output power to the cooling stage with a pulse width modulation. Using the controller software, the temperature ramp/soak schedule was programmed, enforcing condensate formation on the test boards.

Prior to every condensation experiment, the test boards under investigation were placed in the climatic chamber and remained at 25 °C and 92 %RH for an equilibration time of at least 90 minutes. For the purpose of provoking condensing conditions, thereupon the Stage was turned on to gradually reach the theoretical dew point of 23.6 °C. Then the ramp control of the stage was started, cooling down to 22.4 °C in 0.2 °C steps, whereby every ramp and every soak step took six minutes. This is shown schematically in Figure 6.2. The time scales were chosen based on the capability of the Peltier setup to provide a stable cool down without over-or undershooting. The water buildup itself is a dynamic process, thus the idea of stepwise cooling down is to slowly establish different levels of condensate on the PCB surface, while making electrochemical measurements corresponding to each step.

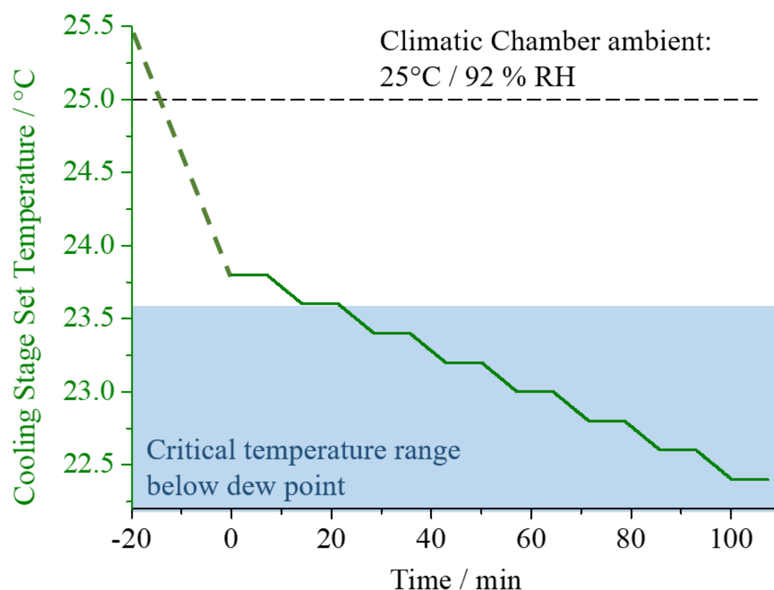

Figure 6.2: Peltier Stage Cooling profile used for provoking condensation on EIS- and Leakage Current-test boards. The blue highlighted area marks the temperature range below the dew point.

D. In-situ camera recording of water film formation

For in-situ observation of the morphology of the water film and subsequent dendrite formation upon DC excitation, a USB Microscope Camera (AM4115ZTL, Dino-Lite) was used. The camera was mounted on a tripod inside the climatic chamber above the test boards on the Peltier Cooling Stage. A USB-connection to the measurement laptop enabled life surveillance of the surface state. The pictures were taken at distinct leakage current measurements values throughout condensation. Whenever the picture of the surface was recorded, it was illuminated using the LED light of the camera, while the light remained off the rest of the time to avoid influence on the controlled condensation.

E. Leakage current measurements and Electrochemical Impedance Spectroscopy

An electrochemical workstation (VSP, BioLogic Science Instruments, France) was used for the DC-leakage current (LC) measurements as well as for the Electrochemical Impedance Spectroscopy. The multichannel potentiostat enables simultaneous EIS and LC measurements. Figure 6.3 shows the schematic surface view of the PCB substrates with two pairs of electrodes for EIS and DC measurements kept on the top of the cooling stage with other attachments. For the leakage current measurements, a DC voltage of 5 V was applied. This potential bias initiates faradaic processes at the electrodes under dewing condition. The course of water adsorption until an established film bridging the gaps as well as the dendrite formation can be related to a leakage current increase, correspondingly a decrease in surface insulation resistance. For EIS

testing, an AC signal amplitude of 10 mV was used. The frequency range was set between 1.3 kHz and 100 kHz. The number of measurement points per decade was chosen to be six, whereby for each of the measured frequencies, five measures per frequency were taken and averaged. For the parallel EIS and DC testing, each for the 200 µm gap and the 300 µm gap samples, three measurement runs were conducted. For each run, new cleaned samples were used.

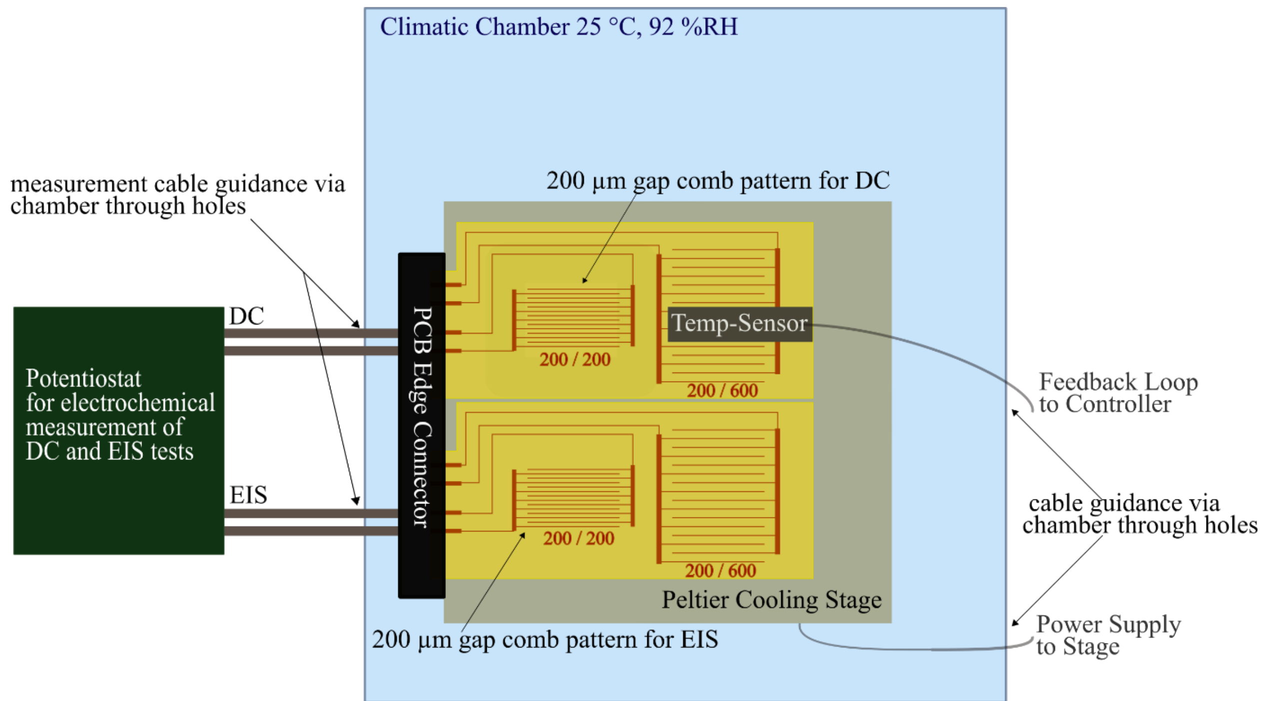

Figure 6.3: Schematic top view representation of measurement setup. Inside of climatic chamber, two identical test PCBs (sketched is 200 µm gap), one for DC and one for EIS measurements are mounted onto Peltier cooling stage. A temperature sensor is fixed to available space on one of the test boards to provide feedback for the control circuitry of the Stage. Cables for controlling and powering the stage, as well as measurement cables of the potentiostat for electrochemical tests are guided outside of the chamber via through holes.

III. RESULTS

A. In-situ visualization of water film buildup

To demonstrate the dew formation until the film visually connects the Cu-Cu-electrodes, the sequential development of the water film was recorded in-situ with a microscope camera on a 300 µm gap comb structure (Figure 6.4). The time *t* given in the pictures in minutes can be compared with the profile shown in Figure 6.2 for temporal overview of water film formation during the ramping profile. At the beginning of the cooling profile at 25°C and 92 %RH, no visible condensation can be seen and the surface of the test boards can still be considered dry (Figure 6.4a) (corresponding impedance is presented later). After 28 minutes (Figure 6.4b), condensation starts in the form of droplet nucleation. The droplets grow larger as

condensation proceeds (Figure 6.4c) and neighboring droplets agglomerate, finally bridging the gap between the copper tracks (Figure 6.4d). It is expected that during the droplet formation, there is an interconnecting layer of water thickness of which changes depending on the undercooling.

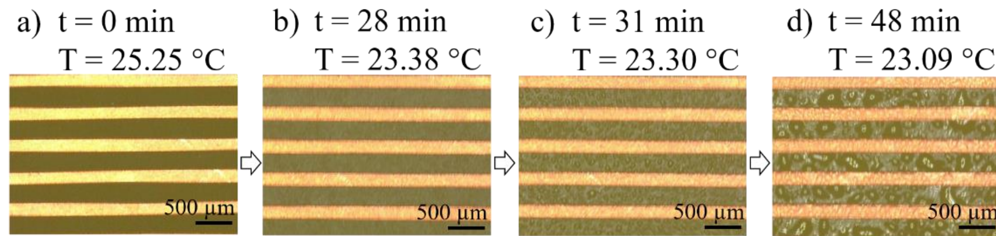

Figure 6.4: Representative micrographs of 300 µm gap copper comb structure before cooling (a) and during cooling profile (b-d). The measured surface temperature at the moment of picture caption is indicated above each picture.

B. Electrochemical Impedance Spectroscopy during condensation

The results of the EIS measurements for 200 µm, as well as 300 µm gap Cu-comb structures show the formation of the water layer in the entire measured frequency range in the form of a drop in impedance |Z| and shift in phase angle towards zero value. The gradual change in the impedance occurs for all the tested samples. Figure 6.5 shows the representative Bode-Plot for just one 200 µm gap structure, recorded over the course of the Peltier stage cooling profile (Figure 6.2). Although a large number of scans were recorded during the experiment, only eight scans within the time frame of 8-62 minutes are shown in Figure 6.5. The Bode Plot gives an exemplary view on the condensation process, starting with formation of small islands until the electrode gap is fully bridged, which is reflected across impedance and phase across the whole frequency range. In dry state, the impedance shows a consistent drop in all of the measured frequencies, starting with > 10^6 Ohm for 1.3 kHz. As the measured frequency increases, the impedance obtains lower values, culminating in 2.5 x 10^4 Ohm for 100 kHz. At this point of scanning, the surface is macroscopically dry, but due to the high humidity ambient, the boards are saturated with humidity and a molecular layer of water is present on the surface. During the progress of condensation (indicated by the green arrow in Figure 6.5), water adsorption is explicitly apparent for smaller frequencies. The scan taken at the moment of most pronounced condensation shows no more evident differentiation in impedance for all measured frequencies. For a connected water film across the gaps, the impedance drops to 688 ± 50 Ohm.

The phase shift in dry state is primarily determined by the laminate for which the surface under dry condition will act as a good electrical insulator between the interdigitated electrode pattern. In accordance with capacitor behavior at high frequency, this results in a phase shift of the test pattern of −87.3° ± 2° in the frequency range between 10 kHz and 100 kHz. As condensation proceeds (displayed by the green arrow in Figure 6.5), the phase shift progressively reaches less negative values. The absolute change is directly

correlated with frequency: For the first stages of water film formation, the largest impact in phase angle change is shown for the lower frequency range. Starting from the fourth displayed cycle, the phase shift at 1.3 kHz does not significantly change, but remains at −27.7° ± 3.8 °. However, the advancing water film buildup can be depicted in the spectrum between 20 kHz and 100 kHz, reaching its least negative value of −3.7° for 31 kHz.

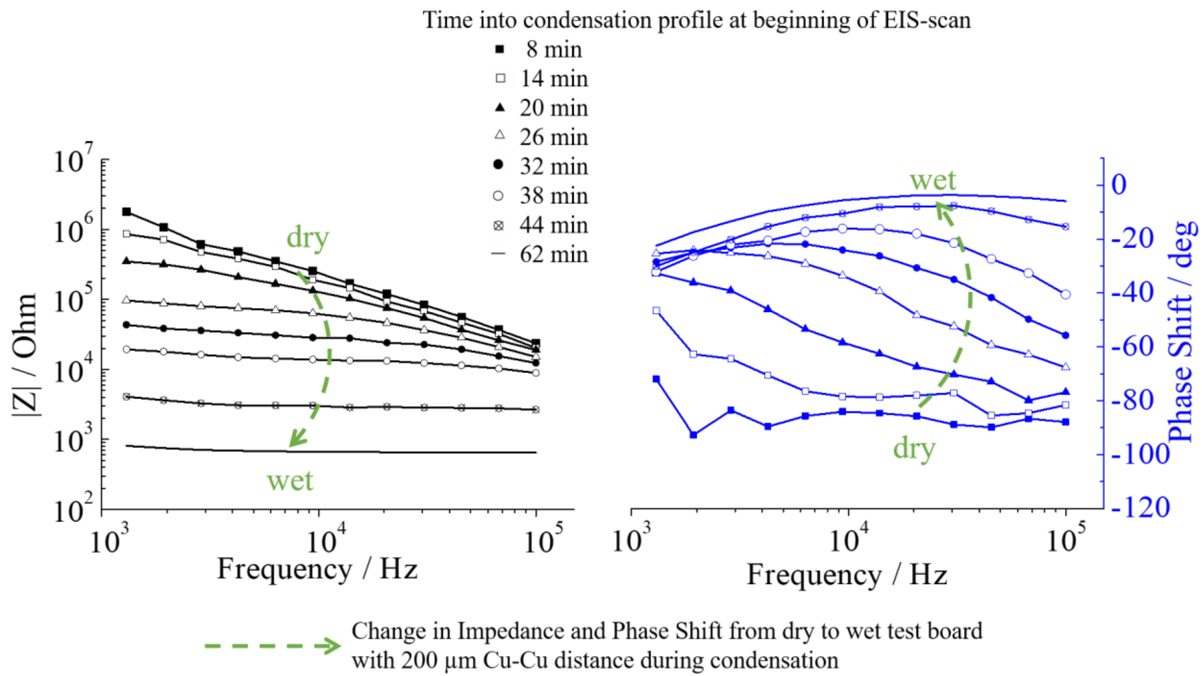

Figure 6.5: Representative EIS scans of a 200 µm copper comb structure during cooling profile at various time intervals corresponding to the cooling profile in Figure 6.2.

Figure 6.6 shows the plot of impedance and phase shift for both gap sizes from the three measurements plotted against various frequencies from each of the conducted measurement runs. This serves the purpose of determining suitable parameters independent of gap size to evaluate the EIS data, also taking into account the level of scatter. This is to be considered in relation to the question of whether a single frequency or range frequencies are better for analyzing the water film buildup instead of using whole frequencies. Two factors are important here: (i) lowest scattering and (ii) higher impedance or phase angle change corresponding to progressive water film buildup. Especially for the phase shift, the lower frequency range is prone to scattering. The higher frequency range is fundamentally more stable and still also exhibits pronounced value change in impedance (minimum of 1 x 10^3 Ohm for 200 µm at 100 kHz) and phase shift going from dry state to having a condensed water layer. On the basis of this, a frequency of 45 kHz (marked with a dashed green line in Figure 6.6) is chosen for further evaluation of the water film monitoring, although a range of frequencies close to 45 kHz can also be used.

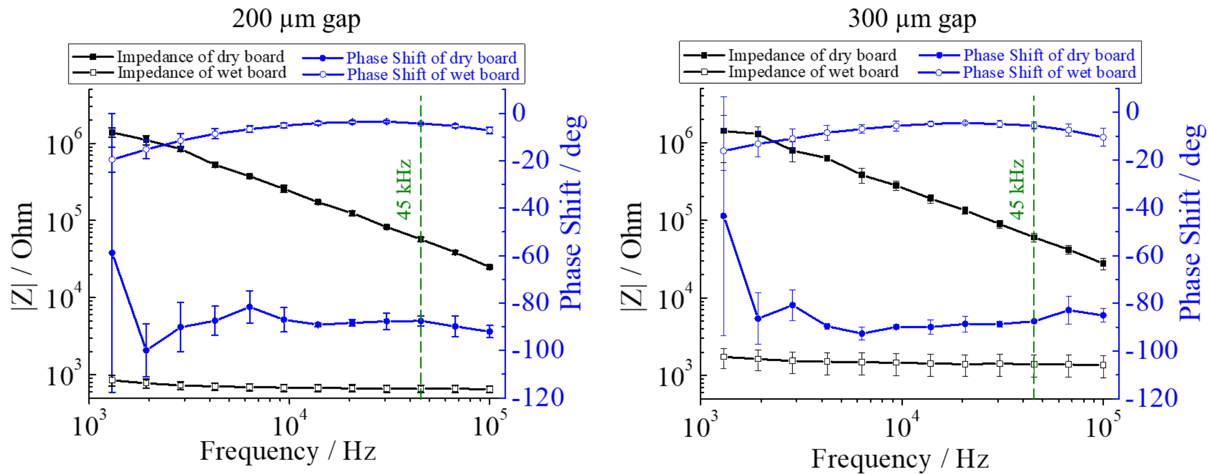

Figure 6.6: Bode plots for dry board (before initiation of cooling profile) and wet board (at lowest point in cooling profile) for 200 µm gap (left) and 300 µm gap (right) test boards. Each of the connected points represents the mean value given with standard deviation for three measurements.

C. Comparison of EIS and leakage current measurements

The EIS measurements were performed in parallel with leakage current measurements to understand the critical level of water film buildup that can trigger ECM with DC bias under transient conditions, where there can be sudden condensate formation on the top of a PCBA. The results of these simultaneous EIS and DC measurements are plotted as a function of time during the condensation process (based on the ramping profile in Figure 6.2). Figure 6.7 shows the data for both 200 µm and 300 µm gap size. For each, three graphs are shown corresponding to three experiment runs. The values of the leakage current measurements (LC, right Y-axis) are shown with the corresponding impedance values |Z| measured at 45 kHz frequency (left Y-axis). Considering the results from DC measurements in Figure 6.7, progression of leakage current shows three regimes. In the range below 1 x 10^{-4} mA, no condensation has taken place and the surface of the test boards can still be considered dry. The current jumps up to a transition regime (associated with currents between 1 x 10^{-4} mA – 1 x 10^{-2} mA), with a slow increase in current. The growth of first dendrites can be depicted by current jumps over 1 x 10^{-2} mA. This shows two extreme failure conditions combining two levels of failures: (i) increased leakage current due to increased water film thickness (1 x 10^{-4} mA – 1 x 10^{-2} mA) and (ii) dendrite formation due to electrochemical migration. The corresponding current level for the dendrite shorting is defined as ≥ 1 x 10^{-2} mA. This level is exceeded in a jump in all conducted tests and has been identified as point of shorting by in-situ microscope recordings of the samples, though not shown here. Thus, these current regimes valid for the test patterns used are referred to “condensation” and “dendrite” in the following.

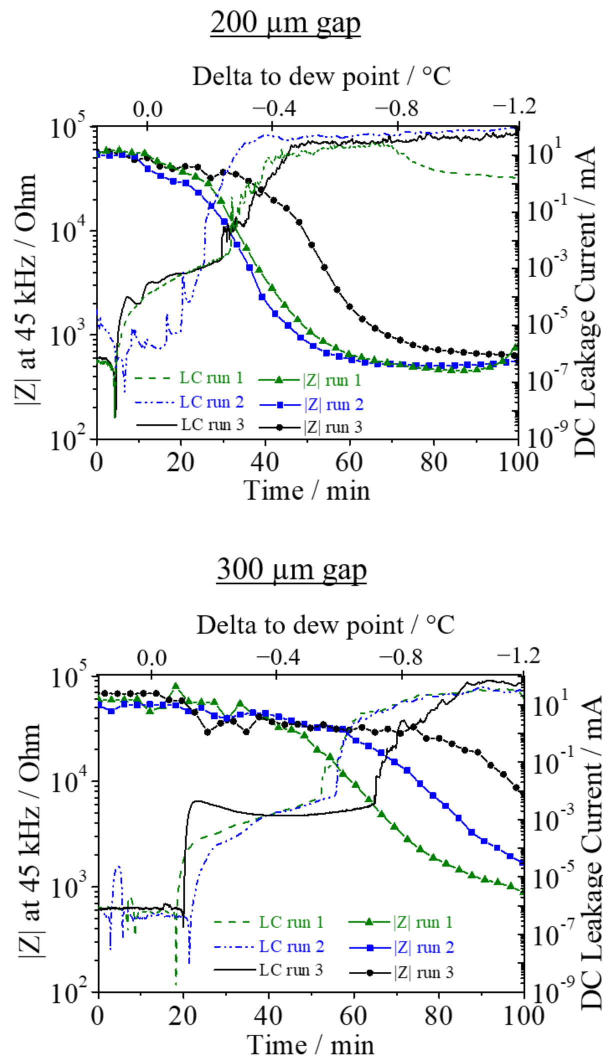

Figure 6.7: Impedance |Z| at 45 kHz and Leakage Current development over the course of the established condensation profile for 200 µm gap test boards (top) and 300 µm gap test boards (bottom) for the each three conducted experiments. The temperature difference from the dew point during cooling is indicated on the top axis.

Looking at the results in more detail, the 200 µm gap DC test boards (Figure 6.7 top) show the previously described leak current progression in a two-step increase. The transition stage shows current value of 1×10^{-4} and 1×10^{-2} mA (~5-25 minutes into the profile). This behavior is especially pronounced in runs 1 and 3, whereas in run 2, the leakage current randomly reduced again for a time frame of approximately three minutes before rising again. All curves exhibit another current increase after approx. 25 minutes, exceeding 1×10^{-2} mA, showing the electrically conducting bridging of the gaps by dendrites. The current level during dendrite formation rises up to 90 mA (run 2) and remains at that level, except for run 1, where it shows a decrease of current towards the end of the experiment. Comparing with the leak current development of the 300 µm gap test boards (Figure 6.7 bottom), the curve progression until ECM occurs is

equally traceable. Though, the time frame for the starting transition range is approximately 20-65 minutes into the profile, thus starting later than for 200 µm and also lasting for a longer period. Results show the gap size dependency on the on-set for leakage current and ECM. For the 300 µm gap, more time is needed for the water to bridge between electrodes and provide a conducting path with required electrical properties.

Considering the impedance of all runs, for both gap sizes, the values exhibit a steady drop over the course of condensation. The first clear reduction for the 200 µm gap test boards is visible after approx. 10 minutes, which is also the time during cooling profile at which the theoretical dew point of 23.6 °C is reached. During stronger condensation, it decreases further until the impedance level reaches a steady value of 500 Ohm. Looking at the progressive evolution of the signal, thickening of the water film up to 65 minutes into the experiment (run 1 and run 2), or 85 minutes (run 3) can be seen changing the impedance signal. However, comparing with the DC measurement, this proceeding water film buildup does not further enhance dendrite growth. As a consequence of these results, it can be assumed that once the impedance has reached a saturation, with bulk water behavior being established, further increase in the water film thickness does not contribute significantly to the electrical behavior.

The results of the EIS measurements of the 300 µm gap (displayed in Figure 6.7 bottom) in terms of impedance show values between 5-6 x 10^4 Ohm in dry state at the beginning of testing. The condensation process is equally traceable by the decrease of impedance, though it occurs delayed compared to the 200 µm gap test boards. The time frame of reducing impedance starts at about 20 minutes into the profile, once the theoretical dew point has already been passed. Although the leakage current transition range progresses between 20 and 65 minutes, a significant change in impedance occurs only after approx. 50 minutes into the profile. At the point of dendrite growth (leakage current $\geq 1 \times 10^{-2}$ mA for DC test board), the impedance has dropped to values between 1 x 10^4 Ohm and 4 x 10^4 Ohm. Unlike for 200 µm gap, at the end of testing, the impedance values have not yet reached steady state values, showing, that the level of condensation is not enough to get the bulk water behavior across the whole test board.

Figure 6.8 shows the comparison of DC measurements and EIS phase shift change with progressive water film buildup for 200 µm gap (top) and 300 µm gap (bottom) size. The phase shift also shows a similar correlation to DC leakage current during water film buildup with a change from −90° in the dry regime up to ≈ 0° under extreme development of water film connecting between the interdigitated electrodes, and formation of ECM in the DC tests. Typical values recorded for 200 µm gap are stable phase shifts of −2° after 60 minutes for run 1 and 2 and 70 minutes for run 3. For the 300 µm gap test board, aside from run 1, the phase shift has not yet reached a saturation level. This once again shows the impact of the gap size on the water film bridging on a PCB surface under condensing conditions.

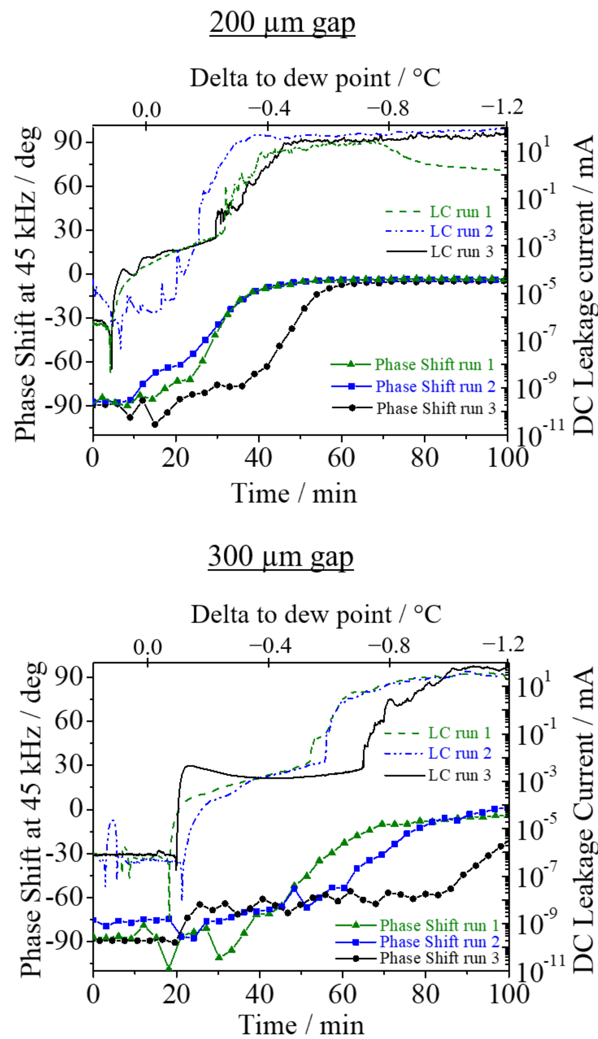

Figure 6.8: Phase Shift at 45 kHz and Leakage Current progression over the course of the established condensation profile for 200 µm gap test boards (top) and 300 µm gap test boards (bottom) for the each three conducted experiments. The temperature difference from the dew point during cooling is indicated on the top axis.

D. Assessment of ECM probability

The conducted DC experiments can be used to ascertain critical states during climatic testing when transient condensation conditions are likely to be established. The combination of DC and EIS measurements combined with the in-situ recording of the surface during the course of the condensation profile, the occurrence of dew formation up to ECM can be distinguished. Leak current levels in the transition range (1×10^{-4} mA – 1×10^{-2} mA) start to show visible condensation on the sample with leak current levels increasing to this level being considered detrimental for electronics in many cases, and a current level higher than 1×10^{-2} mA signifying ECM occurrence. The period of time during the condensation experiments until the specified values are reached are therefore referred to as "time to condensation" (time until leakage

current has reached 1×10^{-4} mA) and “time to dendrite” (time until leakage current has reached 1×10^{-2} mA). Based on the three repeated DC experiments on 200 µm and 300 µm gap (for which the results presented above in Figure 6.7 respectively Figure 6.8), Table 6-1: shows the time to condensation and time to dendrite with standard deviation. The comparison of the gap size effect shows that both time to condensation and dendrite formation increase with gap size, but showing more pronounced effects on dendrite growth (twice as long as the time to condensation). For the 200 µm gap, first condensation is detectable after an average of 14.16 minutes, for 300 µm gap after 22.89 minutes, hence with a delay of 8.73 minutes. The mean time to dendrite for 200 µm is 29.08 minutes, for 300 µm it is 57.81 minutes.

Table 6-1: Time to condensation and time to dendrite for the implemented condensation process on test boards with 200 µm gap and 300 µm gap. The standard deviation is based on data of each three measurements.

Time to condensation		Time to dendrite	
200 µm gap	300 µm gap	200 µm gap	300 µm gap
14.16 ± 5.3 min	22.89 ± 3.5 min	29.08 ± 3.2 min	57.81 ± 6.6 min

The EIS measurements conducted in parallel enables tracking of the dew formation, which is paving the way for electrochemical migration. Hence, a correlation of "condensation"-leakage current (1×10^{-4} mA) and "dendrite"-leakage current (1×10^{-2} mA) is established. Figure 6.9 shows the average phase shift and impedance at 45 kHz with standard deviation corresponding to the these two leak current levels in the DC experiments. Values given for “dry board” refer to data before initiation of the Peltier cooling. The phase shift of the dry test boards and the respective values at the point in time the DC samples reflected the starting condensation process is indistinguishable. The 200 µm gap test boards showed a reduction in mean value, but with a more extensive standard deviation. The mean impedance is reduced by 18.2 % for 200 µm gap and 13.3 % for 300 µm gap. At the time of dendrites bridging the gaps, however, the EIS test boards display a significant drop in impedance and increase in phase angle, which equate the amount of absorbed water needed to enable ECM. For both gap sizes, the EIS values remain in the same range at the moment of dendrite shorting. The phase shift amounts to −52.5 and −59.5 and impedance values to 2.4×10^4 Ohm, respectively 2.7×10^4 Ohm.

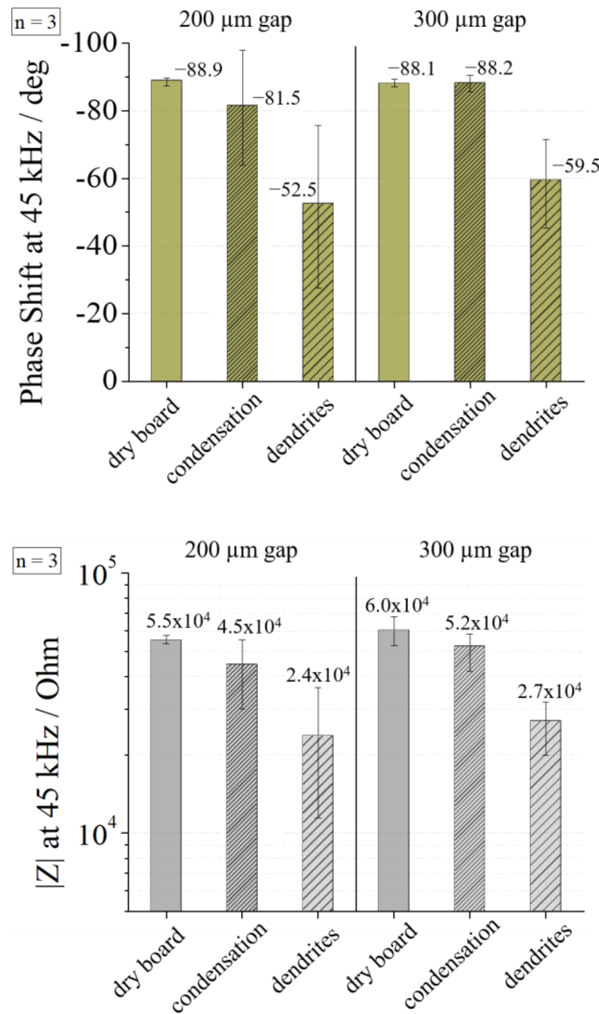

Figure 6.9: Phase Shift (top) and impedance |Z| (bottom) values at 45 kHz obtained from EIS measurements during condensation. “Dry board” shows the values just before the Peltier cooling profile was initiated. “Condensation” shows values corresponding to $1x10^{-4}$ mA in the DC measurement, and “dendrites” shows the value corresponding to $1x10^{-2}$ mA from the parallel DC measurement. Each point represents a mean value with the error bars indicating the minimum and maximum value for the each three measurements

IV. DISCUSSION

Overall the results presented in this paper show the significance of humidity effects on electronics, and how progressive water film buildup under transient conditions leads to failure. In general the results shows that there is a critical level of water film that is required for triggering failure both from the point of view of increased leakage current and electrochemical migration. Transient conditions that occur inside the electronic control units are usually short and depend on the variation in the climate and conditions of the device. Therefore controlling the water film buildup to the critical level during such transient periods is very important for reliability under humid conditions.

Results presented in this paper also show that that the water film buildup can be effectively monitored using EIS, which provides information on the possible onset of higher leakage current or ECM. EIS being a non-destructive technique due to the low applied voltage has more flexibility than the DC measurements as large number of tests can be conducted on one sample without significantly damaging the test PCB.

A. Water film formation and gap size dependence

The condensation process starts with primary nucleation of individual droplets. This happens at the same point in time for both 200 µm and 300 µm gap samples. According to the obtained microscope images as well as other reported work in this area [13], contrary to the assumption that droplet formation starts on the rough FR-4 base material and thus enables capillary condensation, droplets first appear on the metal. Figure 6.10 shows a schematic model of water droplet formation and coalescence, resulting in filling the electrode gap. The droplets forming on the copper are not indicated as they do not contribute to an extent in the closing of the water film in the gap. The growth of nucleated isolated droplets on the base material (see Figure 6.10a)-b)) is proceeding until the drops have grown large enough to touch and coalesce. The newly formed larger drops (Figure 6.10c)) contain the volume sum of the merged drops, though with a reduced surface coverage, resulting in a growth in height. Literature suggests that at this stage, the condensation process has reached a so called “self-similar regime”. In this stage, the system has reached a physical balance between the continuous condensation speeding up to increase in droplet radii and therefore fusion, and the resulting decrease in surface coverage [4, 5]. For this reason, it is a time and gap size dependent process until the dew formation comes to a point were droplets have merged in a way to bridge the Cu-Cu gap. At a point in time when the 200 µm gap boards are bridged by a thin layer of condensate at some position of the comb structure, the 300 µm gap structures are still disconnected due to the statistical process of droplets merging across the larger gap area (Figure 6.10d). Hence, this difference for both of the gaps extends in a way that once the 300 µm gap is finally bridged, the ongoing condensation has already led to a more pronounced water layer in height as well as in places across the 200 µm gap (Figure 6.10e)). Results show the importance of higher pitch distances on a PCB design, which can delay humidity related failures under transient condensing conditions resisting the water film buildup to the critical level.

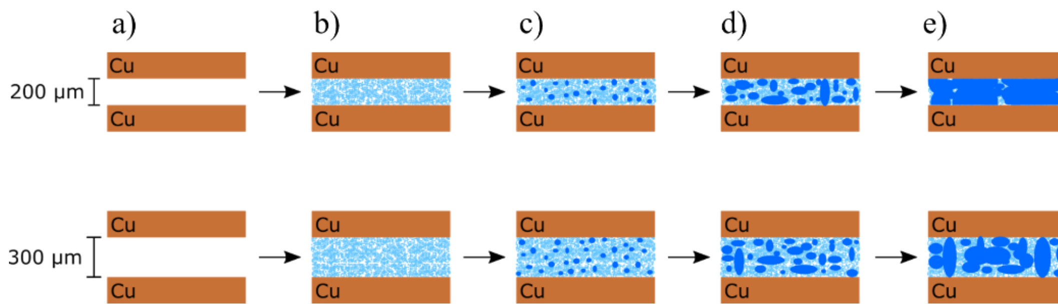

Figure 6.10: Schematic representation of the process of water film closing over the course of condensation for 200 µm and 300 µm Cu-Cu gap.

B. Use of EIS to monitor water film growth

The EIS experiments conducted up to condensing conditions showed that the method is very much suitable to detect the gradual water adsorption until film formation. The idea of thin electrolyte layer`s influence on the impedance has been used in various studies related to humidity concerning reliability of electronics in connection with impact of solder flux activators such as weak organic acids (WOAs) on water adsorption [26] or in relation with the atmospheric corrosion on PCBs [11]. The underlying approach is to understand the physico-chemical state of a sample in its surrounding as an electrical equivalent circuit with different electrical components that represent actual interfaces or processes. The water film buildup is supposed to be epitomized by a change in circuit parameters.

In general, the characteristic shift can broadly be related to the change in signal from capacitive character in the dry state to a resistive behaviour upon condensation. The dry state is related to the beginning of EIS scanning, so a point where the sample is in a surrounding of 92 %RH. By preconditioning the sample, the substrate's bulk is saturated with humidity and a molecular water layer is present on the surface. The measured impedance at low frequency in this condition is comparable to open circuit, due to a limitation of measurement capability of the setup. However, the effect of adsorbed water layer can be clearly seen in the high frequency domain, where it corresponds to the variation of capacitance as local RH level on the board changes during condensation experiments. As the water layer starts to form, the response over a wider frequency range becomes more and more pronounced in terms of humidity detection, as the system is now governed by the conductivity of the film. Hence impedance decreases up to three orders of magnitude and phase shifts change towards less negative values. Results presented in this work show that the EIS measurements can be used in combination with DC measurements to track these gradual changes in dew formation to a coalesced film formation in connection with PCBA design elements to predict the possible humidity effects. The effect of the water layer on the impedance response at different frequencies as shown in Figure 6.5 is based on how the combination of resistive and capacitive elements in the system react. This

can be used as an advantage in predicting different scenarios in connection with the water film buildup and subsequent effect on leakage current and ECM formation. Comparing the phase shift scan obtained after 32 minutes into the profile (Figure 6.5) and correlating with the microscope images from Figure 6.4c, it is possible to see that the low kHz-frequencies are more sensitive to illustrate the presence of water in in droplet and merging-droplet form, but not yet having built a continuous path. Further water adsorption until actual path formation is not distinguishable anymore in the low frequency region of the phase shift (c.f. Figure 6.5 starting at 26 minutes), but more significantly it can be observed at frequencies ≥ 10 kHz. Similarly, the impedance shows first major changes to condensing droplets in the lower frequency range, while a further decrease occurs equally in the higher frequencies once the water film buildup becomes more pronounced.

The results show that a range of high frequencies can be effectively used for evaluating the water film buildup at least in connection with humidity effects on PCBs. A frequency value of 45 kHz has therefore been chosen in this work with the aim of comparing the water film buildup characteristics with DC measurements. Upon a comparison of the EIS results (impedance and phase shift) with DC measurements, it is clear that the water film buildup, bridging, and leakage current as well as ECM development depend on the gap size. This shows the importance of PCBA design elements and pitch distances in determining the frequency of transient water film bridging and failure under transient climatic conditions. For the 300 µm samples, therefore the EIS results presented do not show the stable value at the end of testing for all of the runs. This shows the possible delay in achieving the bulk water behaviour under condensation as the pitch distance increases, which is very relevant in connection with the humidity effects on electronics.

There is only limited knowledge on the transition of condensate to bulk water film level. Especially for rough organic substrates like FR-4, where the condensation process always comes with a water absorption of the material as well, this is difficult to determine. A study made on alumina surfaces concludes that even for more than 20 monolayers of water, the electrical conductivity of the layer is still an order of magnitude lower than compared to bulk water [28]. Taking into account the roughness of the substrates used in this work, it can be regarded that a “bulk water” film, meaning a film being independent in its conductivity from continuous vaporization and condensation in the few top layer corresponds to an even larger number of monolayers.

C. Correlation of EIS and DC testing

The parallel EIS and DC leakage current measurements presented in this study show a correlation between critical level of water film buildup and failures such as leakage current and ECM. Since it is a short term effect, the possibility of improving reliability based on this condition is that one could avoid or delay the

transient water film buildup to the critical level. Possible measures are limiting the minimum gap sizes in a critical area or damping the climatic profile in a possible manner by using improved packaging concepts. The transition towards a point were electrochemical migration is enabled happens gradually, as can be seen from the microscope images (Figure 6.4) and leakage current measurements (Figure 6.7 and Figure 6.8). The results obtained suggest that the "transition" regime in leakage current ($\geq 1 \times 10^{-4}$ mA) found in this study, corresponds to the state of increasing droplet coalescence (Figure 6.10c)-d)). The Cu-Cu gap gets bridged in places, but droplet interactions due to further condensation result in the incorporation of new droplets, which frequently shifts the center of mass of a growing droplet. This prevents the condensate from providing a stable gap-bridging water path long enough to allow dendrite formation. Also in the DC tests, the effect of gap size is observed as the 300 µm gap samples enter the transition range in leakage current with a delay compared to the 200 µm sample.

Figure 6.9 shows that the random bridging is detectable not only by DC testing, but also by EIS under condensation conditions. However, the overall surface coverage of water is still low, therefore the EIS results showing the overall capacitive behavior of the test structure has not significantly decreased, although the level of change is frequency dependent. This impact on the detection capability of EIS is prominent in Figure 6.5. While the 45 kHz frequency is adequate to show changes in film formation for determining the critical level required for ECM, the droplet condensation range prior to this point can be better detected at lower frequencies. The leakage current only increases significantly once a dendrite has bridged the gap and provides a conductive pathway, however the time of increase depends on the gap size (Table 6-1).

Similar to other investigations [3], the ECM results show the time to dendrite formation depends on the gap size with about 2.5 minutes for the dendrite start to short circuit for the 300 µm gap size under the applied bias of 5V. As the time to dendrite formation depends on the gap sizes, it can be assumed that the actual rate-determining step is the dissolution of ions and their transport. Ion transport is a function of the applied electrical field $E = U/d$, with U being the applied voltage and d the Cu-Cu distance. The respective larger electric field for the 200 µm gap test board results to a faster dendrite formation added to the faster closing of the water film similar to the effects reported in the literature [24].

When allocating EIS and DC values for the different gap sizes, two aspects need to be taken into account. First, the fact that one sample was used for DC and one sample for EIS has the consequence that a difference of water layer status on both of the samples at the same point in time always comes into play. This affects the allocation of DC and EIS values. Second, for a smaller gap size, the bridging can happen very rapidly if the droplet distribution and merging in the gap allow it or -in some cases- it can take longer time. The

fact that the bridging can happen at different stages is more prominent for small gap sizes. These two effects combined are mirrored in the data scatter in Figure 6.9, that is larger for the 200 µm gap.

Overall, the results show that the condensation process can be monitored by means of EIS measurements and correlated to the events under DC conditions. The simultaneous DC tests have shown that while the ECM occurrence can be detected both by EIS and DC, a gradual ongoing condensation leading to and ECM-enabling film (prior prediction) can be detected only by EIS. This regime prior to the actual dendrite formation is already detectable non-destructively by EIS, which is a significant advantage in connection with humidity testing. While the leakage current curves impede the assessment of a critical limit due to their slow progression in the transition area and sudden jump upon short formation, the steady decrease in EIS-impedance |Z|, respectively increase in phase shift, offer a better determination of critical points. Expressing the results in form of a relative change, the impedance can be used to assess ECM criticality in a way by stating that it drops to 43.6 % of the dry value for 200 µm gap. For 300 µm, the impedance has dropped to 45 % of its dry value when ECM occurs under DC conditions.

The results presented in this paper clearly demonstrate the possibility of using EIS as a non-destructive method to determine the conditions at which a typical PCB design element causes a critical level of water film buildup for ECM failure. Figure 6.11 shows the non-destructive character of the EIS test method comparing the surface morphology of the PCB at the end of the experiment from DC and EIS measurements. The EIS test board do not show appreciable change. The image of the DC board however shows the spot of a dendritic structure, as they are distributed at random spots all across the comb pattern after testing.

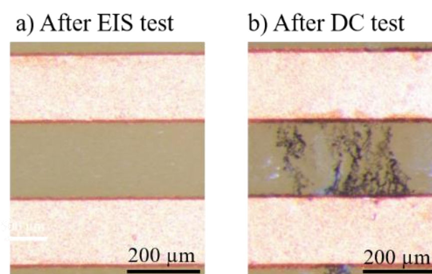

Figure 6.11: Exemplary microscope images from EIS-test board (a) and LC-test board (b) obtained after measurement.

The understanding of the water layer buildup and consecutive changes of the system leading to ECM are key aspects related to the humidity robustness of a PCBA. The power of AC measurements to assess corrosion susceptibility has been used in various studies [14, 17] and contrasted with DC measurements before [31], corresponding in applicability with the results of this study. While the previous work focused

on the determination of electrolyte properties of an already present water film, the presented results show that it is also possible to gradually distinguish the buildup of the electrolyte layer itself. The extensive possibilities and high data content of the EIS technique makes it a valuable tool which can be clearly opted in a broad scope. The outcome of this work can also be regarded relevant for other dew formation related studies aside from electronics, for example for metal corrosion in marine atmosphere or in oil and gas industry.

V. CONCLUSION

1. The optical images obtained during the condensation show that the condensed water film buildup occurs gradual with primary droplet nucleation, local droplet merging, and agglomeration of water film with coalescence to a thicker layer.

2. The results of the EIS measurements for 200 and 300 µm gap Cu-comb structures show the formation of the water layer in the entire measured frequency range in the form of a drop in impedance |Z| and shift in phase angle towards zero value. The gradual change in the impedance at a frequency of 45 kHz has proven suitable to track condensation processes up to formation of a closed water film between interdigital tracks.

3. In the parallel conducted DC Leakage Current measurements, two different current regimes during condensation could be manifested and related to ECM and dendrite formation. For currents between 1×10^{-4} mA – 1×10^{-2} mA, condensate islands are microscopically visible and at the end of the range, ECM is possible. Once first dendrites bridge the gap, the current jumps into the second regime, exceeding 1×10^{-2} mA. The attainment of both regimes depends on the gap size, 200 µm gap samples respond quicker in time than 300 µm and develop ECM first.

4. By comparing EIS and DC Leakage Current tests, specifying a value of EIS-|Z|-drop at 45 kHz to 43.6 % of the dry value for a 200 µm gap test boards and |Z|-drop to 45 % of its dry value for 300 µm gap test boards, a determination of a critical condensation level for ECM was found. With a safety tolerance, it can be stated that the reduction of EIS impedance below 50 % of dry board value signifies dew formation pronounced enough to enable ECM in case of a 5 V DC application.

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7. COMBINED APPROACH OF EIS WITH INTERMITTENT DC TO EVALUATE THE ELECTROCHEMICAL MIGRATION RISK OF PCB TEST BOARDS UNDER CONDENSING CONDITIONS

Simone Lauser, Theresia M. M. Richter, Vadimas Verdingovas, Rajan Ambat

Abstract – This work focuses on the measurement of the initial stages of water film formation on electronics, providing the pathway for electrochemical migration failures. Test structures with interdigitated Cu patterns with varying Cu-Cu-distance and substrate surface such as FR-4 laminate or FR-4 with solder mask were used. Alternating sequences of EIS measurements to trace the water film buildup and DC Current measurements to determine whether the water film was yet pronounced enough to lead to migration were investigated. The results demonstrate that EIS provides insight into the gradual water film formation and consequently predicts dendrite failures non-destructively.

Keywords – electrochemical impedance spectroscopy; surface insulation resistance; water film formation; electronic reliability; humidity, electrochemical migration

I. INTRODUCTION

Miniaturization of electronics, usage of new materials, high-density packing and exposure to various climatic conditions due to increased use has resulted in various humidity robustness issues. The transportation sectors such as automotive, aerospace, and locomotive impose high safety requirements, therefore robustness of electronics over the defined lifetime is important [1]. The challenges in appropriate reliability testing of increasingly complex systems are also indicated by recurring test and field returns [2]. The varying climatic conditions can lead to several failure mechanisms on Printed Circuit Board Assemblies (PCBAs), the key component of common electronics [3]. Depending on the conditions of humidity and temperature exposure, the PCBA surface is prone to thin water film buildup from the dewing processes. Consequent corrosion failure modes can lead to short circuiting of the adjacent conduction tracks or legs of components [1,2]. One of the most frequent corrosion failure types is Electrochemical Migration (ECM). If a water layer bridges two oppositely biased conductors on a PCBA, metal ion dissolution occurs on the positive electrode. Under the circumstance of closely spaced electrodes, dissolved ions will migrate through the electric field via the water layer towards the cathode and deposit. If the water bridge between the electrodes and the voltage bias are maintained long enough, a metal dendrite grows from anode to cathode, short-circuiting the two poles [3]. This will result in intermittent or permanent malfunction of the electronics, depending on whether the current surge through the dendrite is enough to burn to open circuit again.

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ECM is known to occur for various materials such as bare tin, bare copper, tin-based solder and lead or silver [4–8]. Overall the mechanism of ECM is electrochemical in nature, involving metal dissolution and deposition, transport through the solution layer, and local chemistry changes in the solution layer [9]. The fundamental requirement however for ECM to happen is the formation of a water film. The continuity as well as the electrical properties of the film primarily determine the ECM-criticality. Thus, understanding and controlling the water film buildup equates to an understanding of the pathway for ECM occurrence.

The formation of a dew film itself starts with the nucleation of small thermodynamically stable liquid drops on a surface with a temperature that is equal or lower than the dew-point temperature [10]. The rate of nucleation depends greatly on the surface wetting properties. Droplet growth is guided by the concentration gradient of water vapor molecules surrounding the surface of the material [11,12]. Thus, growth kinetics are dependent on the proliferation of this depletion zone. In addition, the possibility of transferring the heat of condensation into the substrate was shown to have an influence. If this is not easily given, the temperature of the drop rises, consequently slowing down its growth or even stopping it [12].

Considering an array of separated droplets, the separate vapor concentration profiles can be regarded as an interlinked film, only altering in the direction normal to the substrate plane. Once droplets have grown large enough to touch each other, they coalesce. In this condition, the system is found in a state of constant surface coverage. This is established for two reasons: (i) As condensation proceeds, the individual droplet radii rise. (ii) Simultaneously, the associated increase in coalescence events leads to the fact that through merging, surface area is set free. This is because upon combining various single droplet volumes into one, the new droplet grows in height, hence receding on the substrate surface [12–14]. On the released area, new droplets can form, making up a new droplet generation, that grows with an individual rate [15]. As coalescence proceeds, the emerging droplets grow larger in plane as well as in height, passing to a thin water film status. The impact of such a dew formation process in terms of corrosion of electronics has been recognized and partially investigated. Saline contamination, similar as found on electronics situated close to marine atmosphere, was shown to enhance corrosion. Due to the hygroscopicity of the salt, the dewing process is facilitated. As the salt dissolves into the water film, it provides increased conductivity and accelerates the corrosive processes [16]. For electronic components such as for a PCBA, surface contamination other than salt is possible due to the presence of retained chemistries from various processes steps, for example soldering [17,18].

When considering ECM as corrosion phenomenon, the understanding of the water film formation is essential when wanting to comprehend the synergy between water film buildup, start of faradaic reactions, and finally dendrite formation. Today, PCBA surfaces with regard to their humidity robustness and

propensity for ECM are tested using DC voltage. One of the most common methods is the Surface Insulation Resistance (SIR) test. This method is based on the principle of resistance measurement between two electrically conducting materials. These can be the patterns or components terminals on a PCBA, between which a voltage is applied. The measured SIR across the electrode gap is a result of four pathways: (i) air, (ii) surface, (iii) surface contamination, and (iv) substrate. For a standard PCB-surface, this approach can be simplified to considering substrate (bulk conduction) and surface effects (general water adsorption and contamination impact on condensation). Hence, formation of a water layer and consequently electrochemical migration are both the processes with significant impact on the measured SIR values. Once a distinct water bridge is formed between the contacts and a certain potential is applied, an ionic current can be established across the gap. The progressing chemical reactions can subsequently lead to the formation of the dendrite. This results in a rise in leakage current, hence a drop in SIR [19,20]. The DC based techniques have been used to evaluate humidity effects on electronic assemblies in various scenarios. These include the impact of different contamination emerging from no-clean flux systems on ECM [21,22] or the durability of conformal coatings as encapsulation for MEMS devices [23]. A major drawback of DC methods like SIR testing is the fact that the gradual buildup of dew until a closed water bridge is formed between contacts cannot be distinguished in detail. The application of the DC potential (typically 50-100 V) leads to dendrite formation, hence the failure to be detected. However, the polarization of the electrodes that is accompanied with the bias, prevents the method from detecting successive condensation if a constant potential is applied during the measurement [24]. Therefore, an understanding of the level of humidity on a PCB surface prior to failure is difficult to obtain with DC methods.

Instead of the DC approach, techniques based on the application of an alternating voltage, such as Electrochemical Impedance Spectroscopy (EIS), can be used. A test sample comprised of two electrodes is excited with a low amplitude AC-voltage in the form of a sinusoidal wave implying different frequencies. The response towards this excitation describes the state of the system. Obtained data can be represented and evaluated in various ways, depending on the parameters to be analyzed. One of the options is to evaluate the impedance |Z| or the phase shift for the tested frequency spectrum (Bode Plot) or only for distinct frequencies. Another approach is to regard the investigated system as circuit of electrical equivalents, each of them representing typical characteristics of the system under investigation. Fitting the data to an appropriate equivalent circuit serves the purpose of gaining a model understanding of the system [25,26].

In the context of water film formation on a PCB surface, changes in resistive and capacitive properties of the system in general can describe the water layer buildup between metals acting as electrodes. The principle of this approach is the same as for most commercial humidity sensors i.e. absorption of humidity changes the conductivity or the dielectric behavior of the electrode system. This results in a measureable

change that can be related to a distinct humidity [27]. In the context of corrosion evaluation, the EIS method has been used to evaluate atmospheric corrosion of steels and copper by performing measurements on samples covered with thin electrolyte layers [28]. It was also employed to compare the corrosiveness of different fluxes and related to DC testing in the assessment of critical flux residues in high humidity environment [29,30].

However, in order to use EIS as a method for monitoring humidity robustness of PCBAs and to predict ECM failure, a comparative study of the EIS and traditional DC methods is required. Studies in the literature used either EIS or DC methods to investigate the humidity effects. The EIS test method as an alternative to DC is not investigated in detail. Using EIS as a humidity robustness test method can be very advantageous due to the non-destructive character of the method compared to DC testing, which can cause irreversible dendrite formation. It is also important to note that many humidity related failures are due to the transient water film buildup on the PCBA surface under condensing conditions, which last only for a short period time. Therefore, the humidity robustness of the PCBA is determined by its ability to withstand substantial levels of water film, which result in facilitated electrochemical processes and ECM. If one can detect the PCB characteristics influence on transient water film buildup using EIS and possible effect under DC conditions can be extrapolated, this gives a huge benefit. The EIS tests can be repeated easily without using a large number of boards (due to the non-destructive nature) and time of testing can be significantly reduced.

Present paper focus on correlating the traditional DC method used for evaluating the humidity robustness of PCB samples with EIS. The main objective is the general evaluation of usefulness in terms of monitoring the gradual transient water film buildup and its consequence to ECM failure. Studies carried out include combined study of EIS and DC leakage current experiments to compare the techniques with the possibility of using EIS as an alternative method for evaluating PCB reliability towards humidity. The aim of this approach is to comprehend in much more detail the condensation status enabling ECM. Accordingly, both methods are used in an alternating manner on one PCB board. By means of EIS, the gradual condensation is detected electrically. Intermittent application of a DC potential promotes ECM if a water path is established. By facilitating the measurement of the water bridge buildup and correlating this process with the occurrence of ECM, a theoretical insight as well as a possibility of non-destructive reliability testing are aimed for. PCB samples with Cu-traces of different gap sizes and gap surface materials are driven into condensing conditions. This is achieved by reducing the surface temperature below the dew point in a controlled climatic environment of 25 °C and 92 %rH. EIS and DC are evaluated in comparative manner to determine an ECM-critical water film by EIS.

II. MATERIALS AND METHODS

A. Test Boards

The combined EIS and DC tests were performed on SIR copper comb test patterns. The design is based on IPC-B-25 standardized test boards. Three different boards were used. They differed in separation distance of interdigitated electrodes and in substrate surface. The thickness of the test boards corresponded to 1.6 mm. Test boards contained one or two comb structures with interdigitated distance of 100, 200, and 300 µm with one of the 200 µm comb patterns applied on the solder mask surface (Figure 7.1b)), while the other directly on the FR-4 surface (Figure 7.1a) and c)). The Cu width in the comb area was 200 µm for all structures. For a complementary analysis of condensation along with in-situ camera recordings, one 200 µm Cu-Cu distance sample on FR-4 (like displayed in Figure 7.1a)). was used, but cut to a smaller size to allow camera recording of the whole measured structure. All of the test boards were cleaned thoroughly prior to testing. The cleaning bath consisted of 75% Isopropyl alcohol and 25% DI-water, and was kept at 45 °C (based on IPC-TM-650, Method 2.3.25). The samples were exposed to the cleaning solution for 20 minutes. In order to give enough time for subsequent drying, they were stored in a dessicator filled with silica gel for a duration of at least 14 hours after the cleaning procedure.

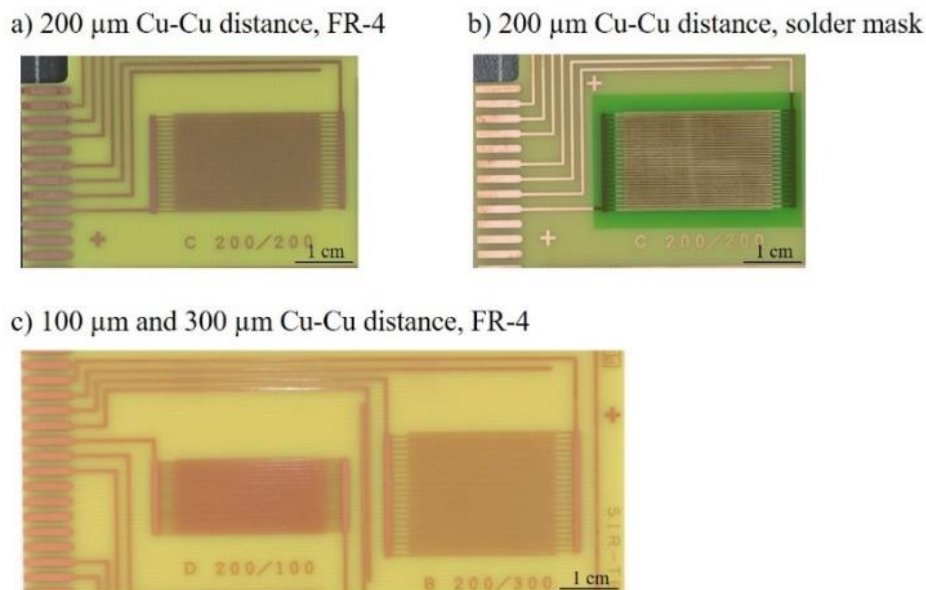


Figure 7.1: Test boards with one Cu comb structure of 200 µm width and Cu-Cu distance of 200 µm (a, b) and test board with two Cu comb structures of 100 and 300 µm Cu-Cu distances. Substrate surface is FR-4 for (a, c) and solder mask for (b).

B. Climatic Conditions for Condensation Experiments

The electrochemical measurements were performed in an “Espec PL-3 J” environmental test chamber (ESPEC Corp., Japan). The chamber has the capability for temperature cycling between −40 °C and 150 °C and relative humidity (RH) between 20 % and 98 %. For this investigation, the climatic chamber was used to provide a stable ambient for the systematic condensation tests. The settings of the chamber were 25 °C and 92 %RH.

To enable condensing conditions on the surface of the test boards, active cooling of the samples triggered local water adsorption. This was achieved with a cooling stage with embedded Peltier elements (CP-031, TE Technology Inc., USA). The schematic of the setup used for condensation is shown in Figure 7.2.

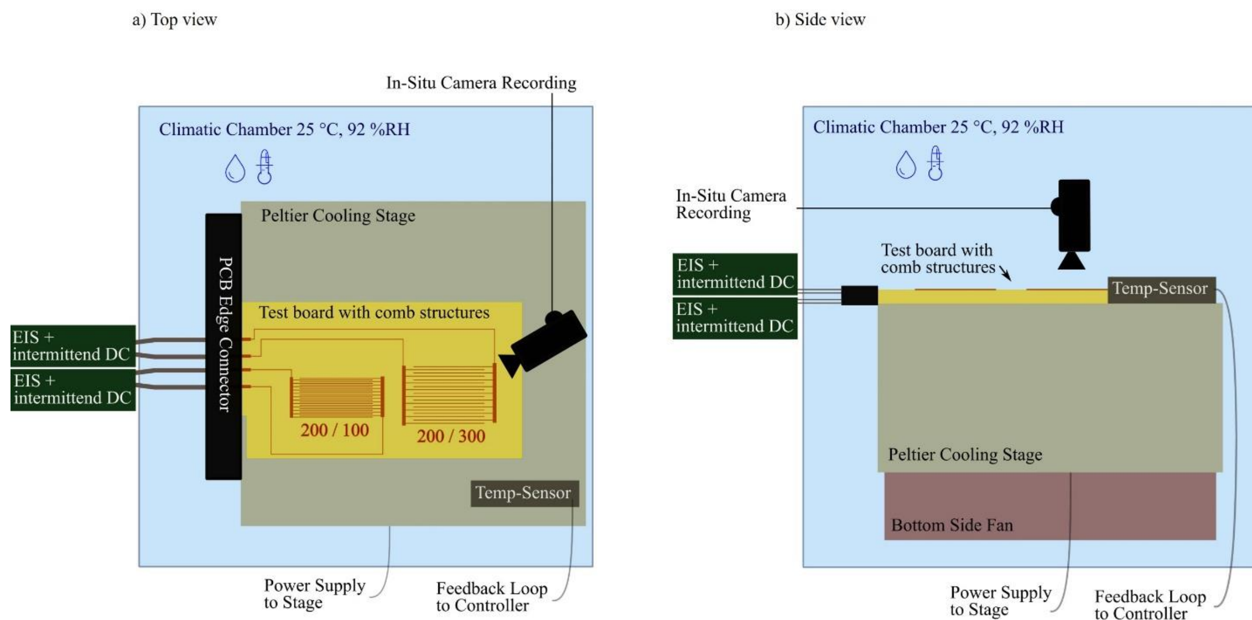


Figure 7.2: Schematic top view (a) and side view (b) of measurement setup comprising the test board mounted on the Peltier Cooling Stage within the climatic chamber, providing a stable surrounding climate.

The test boards were placed on the stage by means of a heat conducting paste (Non-Silicone Heat Transfer Compound, Electrolube, UK). The power to the stage was applied by a separate DC power supply, as was the bottom-side fan to dissipate the heat generated by the Peltier elements. With a separately powered controller (Heat & Cool Bipolar Controller TC-720 OEM, TE Technology Inc., USA), the output power to the cooling stage was regulated to a cooling profile, programmed via the controller software. A temperature sensor (MP-3139, TE Technology Inc., USA) fixed to the setup provided the temperature status needed for a feedback loop to the controller.

After mounting to the cooling stage, the samples were kept at 25 °C and 92 %rH for the 90 minutes before testing was started. This interval was given to stabilize the climate and for the samples to absorb humidity in order to minimize the absorption impact on the subsequently provoked condensation.

To induce condensing conditions, a temperature ramp/soak cooling profile was used. The theoretical dew point at the imposed ambient temperature and humidity of 25 °C and 92 %rH amounts to 23.6 °C. The temperature was fast first brought down to 23.8 °C within 60 minutes, then further reduced in 0.2 °C steps, whereas each ramp and soak step took 60 minutes (see Figure 7.3)

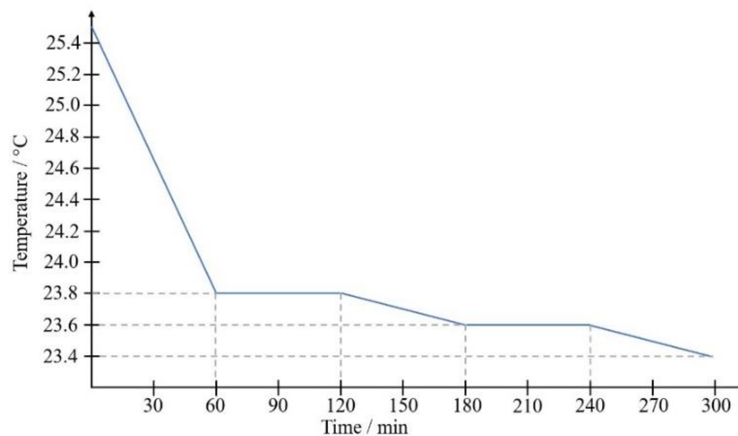


Figure 7.3: Peltier Cooling Stage Temperature Profile used to provoke condensation on test boards.

A high-resolution imaging camera (AM4115ZTL, Dino-Lite) was placed inside the climatic chamber in order to provide complementary in-situ recording of the dew formation. The USB connection to the measurement laptop allowed temporarily turning on of the LED-illumination and taking pictures during the condensation and the ECM-process.

C. Electrochemical Impedance Spectroscopy and DC Leakage Current Measurements

Electrochemical Impedance Spectroscopy and DC-Leakage Current tests were performed to assess the ECM-critical transition points during condensation. An electrochemical workstation (VSP, BioLogic Science Instruments, France) enabling both measurement modes was used. The DC bias promoted ECM processes between the Cu-electrodes once enough condensate had formed in between them. EIS measurements were used to follow the gradual buildup of this water layer. In order to provide the best possible correlation of non-destructive EIS and dendrite-promoting DC measurements, both of the techniques were performed alternatingly on each test structure in the two-electrode-setup (Figure 7.4). In between DC and AC measurements, there was a 30 s wait period (not shown in Figure 7.4) without AC or DC potential. This was done to ensure the removal of any polarization effects during the DC sequences.

EIS measurements were performed with an AC excitation voltage of 10 mV, with a range of frequency from 10 kHz to 100 kHz in logarithmic spacing. This narrow frequency range was chosen intentionally in order to provide brief measurement sequences during the momentary condensation course. For each frequency, five values were taken and averaged. After approx. three minutes of EIS measurement, a 5 V DC bias for 300 µm Cu-Cu gap and respectively 1.667 V for 100 µm Cu-Cu gap was applied to the test structures and the leakage current was measured. Adjustment of the voltage in this case was done in order to tests both structures under the same electric field. 200 µm structures were measured at 5 V.

If a distinct amount of water was present on the surface between the traces during a DC-step, the voltage lead to the formation of dendrites bridging the gap due to ECM. If no ECM-enabling water path was provided on the surface yet, the potential was shut off again after three minutes and another EIS measurement was conducted. This periodic approach was prolonged during ongoing condensation until the formation of closed dendrites took place in a DC step (indicated by current > 1 x 10^{-2} mA). By evaluating the EIS values from the previous step, a correlation between EIS information and ECM in a DC case was made.

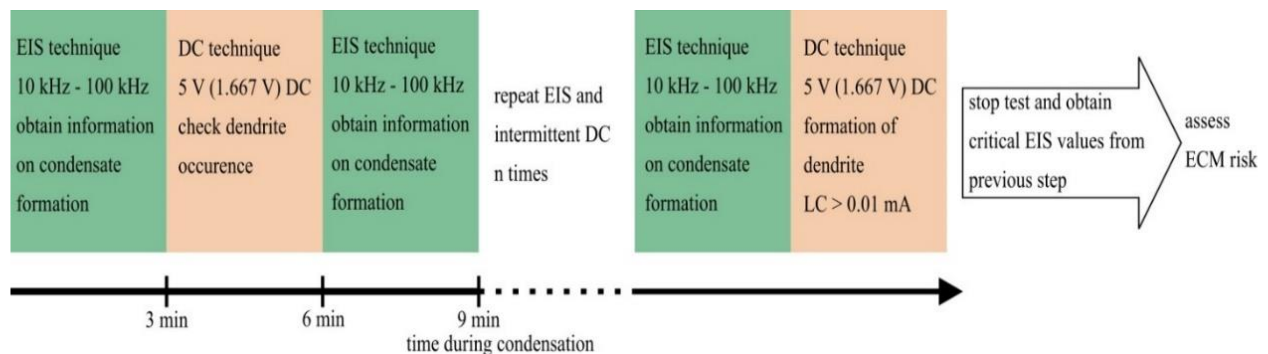


Figure 7.4: Representation of combined EIS and DC approach to assess water film status enabling electrochemical migration. EIS was conducted in a frequency range between 10 kHz and 100 kHz. During DC sequences, the applied voltage was 5 V for 200 and 300 µm gap samples and 1.667 V for the 100 µm gap samples.

This approach was applied in four different experimental series with three to seven runs with each new samples (see Table 7-1). Each of them enabled a DC and EIS correlation. For all four experiment series, the same cooling profile was used, however, for series C and D, the condensation process was prolonged compared to A and B. This was achieved by means of the Peltier regulating thermistor. For experiment series A and B, the thermistor was fixed to the test board's surface. For series C and D, the sensor was mounted onto the stage itself, as displayed in Figure 7.2. This way, for series C and D, a more pronounced cooling impact was needed to reach the dew point temperature also on the board, hence it required longer time.

Table 7-1: Overview of the conducted experiments with information on gap material, gap size, applied electrical field and repetition runs.

Experiment series	Gap material	Gap size in µm	DC electrical field in V/m	repetitions
A	FR-4	200	25.000	3
B	Solder mask	200	25.000	3
C	FR-4	100	16.670	7
D	FR-4	300	16.670	7

D. Gravimetric measurements

For an approximate quantification of water amount on the PCB surface under various conditions, complementary gravimetric measurements were performed. A highly absorbing tissue paper was cut to the area of a 300 µm gap size comb structure (5.25 cm^2). The tissue was used for removing the condensed water from the surface in order to determine the quantity by weighing. These gravimetric measurements were performed with each new samples five times for getting approximate water amount for: (i) “condensation” region (leakage current exceeding 1 x 10^{-4} mA) and (ii) “dendrites” region (leakage current exceeding 1 x 10^{-2} mA). The tissue was weighed in its dry state, and then pressed to the surface area of the comb to absorb the condensed water. By weighing the wet tissue again and subtracting the dry tissue weight, the approximate level of water load on the surface was calculated.

III. RESULTS

A. Correlation of AC and DC measurements during water film buildup together with in-situ imaging

In order to establish a correlation of electrochemical measurement and water status on the surface, AC and DC measurements were performed over the course of condensation along with in-situ camera recordings. The results were evaluated chronologically. This experiment was conducted in order to form the basis for the further experiments by evaluating the formation of water using a smaller interdigitated pattern so that entire surface could be observed in-situ as described in the experimental section (gap size 200 µm). To show the impact of the condensation on the measured frequency spectra, Bode plot representation is given for $t1$ = 0 min, $t2$ = 50 min, $t3$ = 60 min and $t4$ = 70 min during the climatic profile (Figure 7.5).

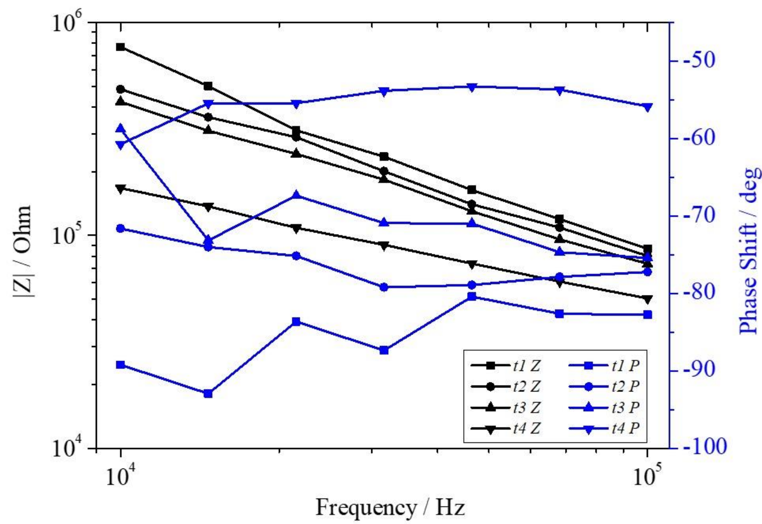


Figure 7.5: Exemplary full spectra of impedance (Z) and phase shift (P) from t1 = 0 min, t2 = 50 min, t3 = 60 min and t4 = 70 min during condensation.

It is shown that impedance (|*Z*/) decreases over the regarded frequency spectrum. Phase shift (*P*) changes from the range of -90° towards less negative values, with the most stable range of this transition being in the higher frequency region. The data shows that generally the complete measured frequency range could be used to trace the water film buildup on the sample surface. However, as the higher frequency range shows the most stable progression from dry to wet status, 68 kHz frequency was chosen for further specific analysis in this paper. The selected frequency represents the high frequency domain for which the transition from capacitive response to resistive response occurs when water condenses on the surface of the board. The EIS data shows that for both impedance and phase shift at this frequency, the changes during water film buildup are pronounced.

Figure 7.6 shows the results of EIS corresponding to the 68 kHz frequency extracted from the full spectra. The leakage current from the intermittent DC testing is plotted additionally. The alignment of data with the microscope images shows that the buildup of the water film until dendrite growth can be retraced from both impedance and phase shift of the EIS as well as the DC leakage current.

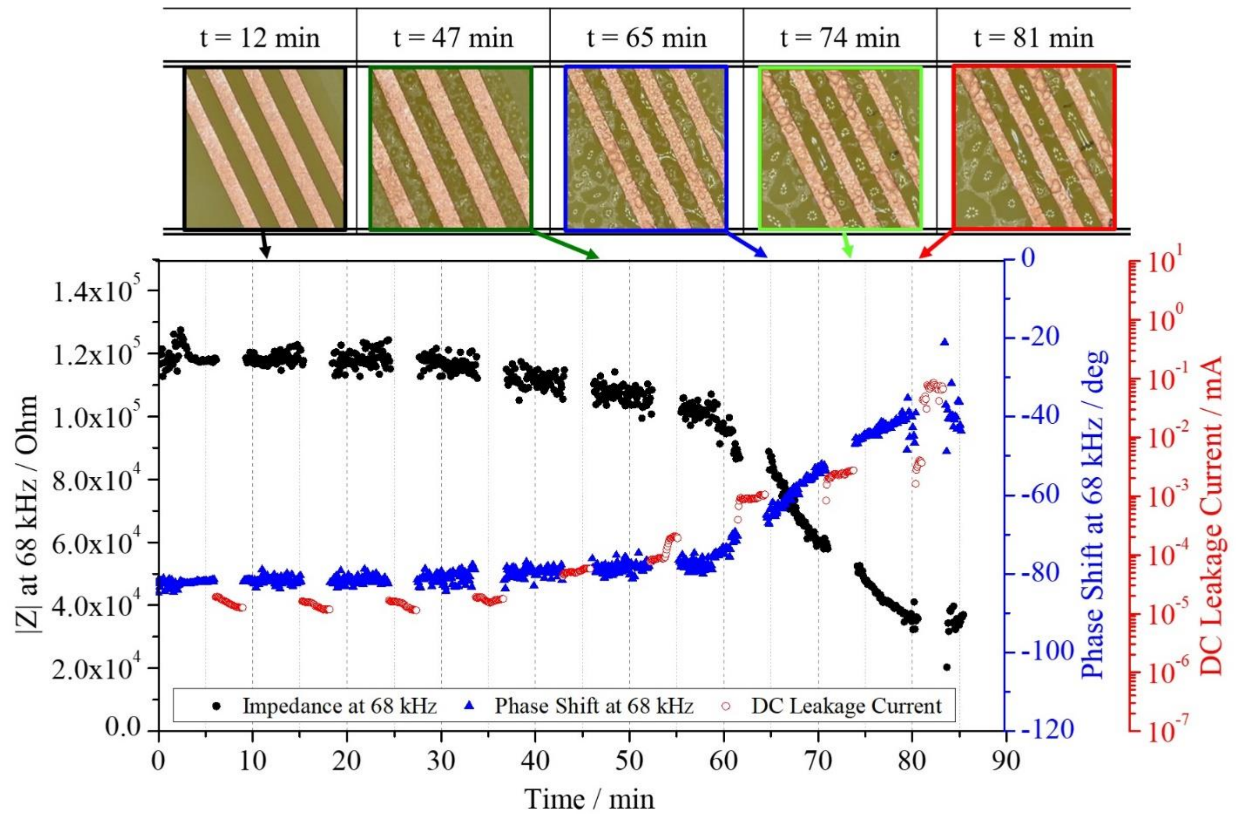


Figure 7.6: EIS impdance and phase shift @ 68 kHz and DC Leakage Current recorded during the progressive condensation of the sample. Recorded microscope images show the respective surface state of the sample at distinct points during condensation to ECM formation.

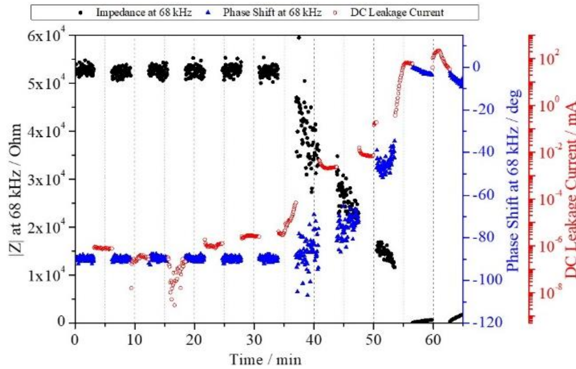
The start of dew formation is seen in the EIS signal by showing a slight impedance decrease after approx. 30 minutes. After 47 minutes into cooling, the microscope camera shows clear droplet formation between the Cu-traces. This is reflected in the measurement by a further impedance reduction, and a phase shift increase towards −75°. At this point, the DC leakage current shows significant increase. After 65 minutes, the image shows visible bridging of the Cu-Cu gap at various points on the test board. The impedance has reduced significantly below 8 x 10^4 Ohm and the phase shift has dropped to −60°. The intermittent DC measurement at this stage showed leakage current levels exceeding 1 x 10^{-4} mA. The in-situ image corresponding to 74 minutes shows more pronounced level of water film buildup. Starting dendrite growth between the tracks can also be recognized. The larger water load is reflected in further gradual decrease of impedance. The increasing resistive nature of the system that the water bridges establish is also mirrored in the less negative phase shift (approx. −40°). During the DC-period starting at 80 minutes into cooling, the dendrite can be observed to bridge the gap. This results in an immediate increase in leak current to 1 x 10^{-2}mA (81 minutes).

B. EIS and DC signal evolvement during condensation on SIR PCB with various electrode distances

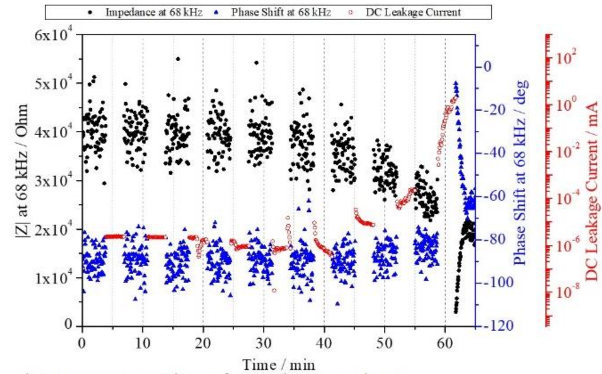
Based on the results presented in Figure 7.5 and Figure 7.6, a series of EIS and measurements were conducted on SIR comb structures with different electrode distances, mimicking common PCB pitch distances. The EIS and DC measurements were performed alternatingly during progressive Peltier cooling profile (Figure 7.3) with all samples in the experiment series A-D as described in Table 7-1. For each of the series, results of one exemplary run are displayed in Figure 7.7. EIS data is represented as impedance and phase shift at a frequency of 68 kHz and is plotted along with the DC leakage current. Full EIS spectra corresponds to each of these experiments was collected similar to that shown in Figure 7.5, however not shown.

For all experiments in this series, the progression of impedance (black) and phase shift (blue) show the course of water film formation by impedance decrease and phase shift change towards less negative values. Likewise, the intermittently performed DC sequences (red) show the condensation up to dendrite formation by a current increase. It is recognizable for all series, that the EIS signal progresses in a steady manner during condensation, while the leakage current undergoes distinct regimes of slower and faster rising. All the experiments (A-D) showed similar correlation between EIS and DC, similar to that explained for Figure 7.6, thus with possible predictability. Although the time interval is different depending on the pitch distance, the impedance value reaches close to $2.2 \cdot 10^4$ Ohm corresponding to the DC measurement showing ECM.

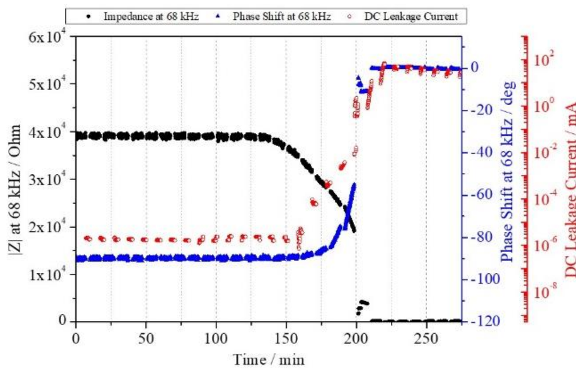
a) Measurement data of experiment series A
gap material: FR-4, gap size: 200 µm



b) Measurement data of experiment series B
gap material: Solder mask, gap size: 200 µm



c) Measurement data of experiment series C
gap material: FR-4, gap size: 100 µm



d) Measurement data of experiment series D
gap material: FR-4, gap size: 300 µm

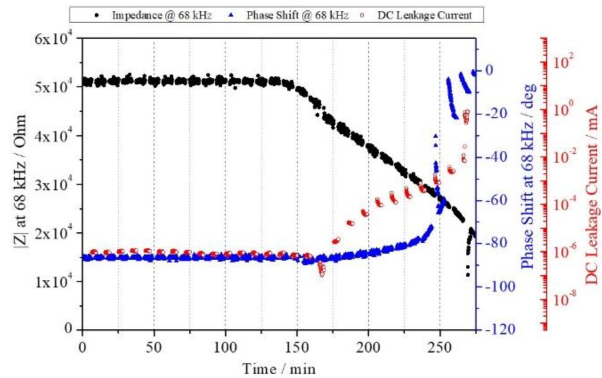


Figure 7.7: Representative results of EIS impdance and phase shift @ 68 kHz and DC Leakage Current measurements recorded alternatingly during Peltier cooling. Shown are experiments of series A (a)), B (b)), C (c)) and D (d)).

Series A result shown in Figure 7.7a) corresponds to a comb structure of 200 µm Cu-Cu gap on FR-4 laminate. The progressing condensation is observable with an impedance decrease from 5.3 x 10^4 Ohm down to 3 x 10^4 Ohm after 35 minutes and a change in phase angle. The leakage current starts to increase to a plateau range in the prior step and remains at approx. 1 x 10^{-3} mA until 50 minutes of time. At this point, a current of 1 x 10^{-2} mA is first time exceeded, attributed to dendrite formation. The EIS values from the previous AC step represent this ECM-critical water film by and impedance of $2.2 \cdot 10^4$ Ohm and a phase shift of −70°.

Figure 7.7b) shows results of measurement series B (200 µm Cu-Cu with solder mask surface in gap). The condensation process up to ECM and formation of gap-bridging dendrites can be equally retraced. The decrease in impedance and increase in phase shift is trackable as in the previous case together with an increase DC leakage current. The phase shift data contains some noise in this case. The impedance is able to retrace the water film buildup despite scattering and has reduced to approx. 2.5 x 10^4 Ohm before dendrite formation during the DC step after about 60 minutes.

Typical data from experiment series C (100 µm Cu-Cu traces, FR-4) is displayed in Figure 7.7c). Compared to measurement series A and B, condensation occurs at a later stage during Peltier cooling. This is because the thermistor used for regulation was mounted not on the sample itself, but on the stage, therefore cooling is slower. The first visible signs of dew formation are displayed in the EIS signal after approx. 140 minutes. With time, impedance continues to decrease as the leakage current and phase shift start to increase. After 200 minutes, a sufficient amount of water has condensed to enable formation of a closed dendrite. Although the water film buildup is slower for this set of experiments, the amount of water that represents the possibility of dendrite failure is similar to that observed in the other experiments: by an impedance of 2 x 10^4 Ohm and phase shift of −55°.

Data shown in Figure 7.7d) corresponds to 300 µm gap samples on FR-4 (series D), with the cooling carried out similar to series C. After 150 minutes, the impedance starts to decrease steadily, while the DC measurement reaction to the condensation is about 20 minutes delayed. As the transition area in which the current slowly increases up to 1 x 10^{-2} mA passes, the impedance significantly decreases further and the phase shift rises after 200 minutes. Once the formation of a closed dendrite occurs after 220 minutes, the characteristic of the water film formed can be described by the EIS values of 2.1 x 10^4 Ohm and a phase shift of −22°.

C. Evaluation of EIS-measurement for ECM risk

The conducted experiments of series A-D were evaluated in terms of ECM criticality related to the EIS data. For this purpose, the impedance values at 68 kHz frequency were evaluated at different stages during testing. For each series, mean impedance values were calculated for “dry” state, “condensation” and “dendrites”. The dry state corresponds to the impedance values before Peltier cooling was initiated. Condensation stage refers to the impedance values prior to the DC sequence in which the current exceeded 1 x 10^{-4} mA. Likewise, ‘dendrites” shows the impedance right before the step in which dendrite formation occurred under DC bias (corresponding to a current ≥ 1 x10^{-2} mA).

The results in Figure 7.8 show mean impedance values with minima and maxima for *n* number of experiments for all stages. For all test boards, an impedance decrease from dry state to “condensation” and further to “dendrite” state can be found. For samples with 200 µm Cu-Cu gap and FR-4 gap material (series A, grey checkered), the mean dry state impedance amounts to 5.2 x 10^4 Ohm. In the EIS-sequence before “condensation” current is reached, the impedance has dropped to 3.4 x 10^4 Ohm. Right before dendrite shorting, the value reached is 2.2 x 10^4 Ohm on average, meaning that the value has been more than halved compared to the dry surface. Comb structures with solder mask in between gaps (series B, green cross-striped) exhibit a dry state value of 4.0 x 10^4 Ohm and drop to 2.8 x 10^4 Ohm before leakage

currents ≥ 1 x 10^{-4} mA are reached in the following DC-sequence. The impedance marking a water film status that enables closed dendrites upon DC application has a mean value of 2.2 x 10^4 Ohm.

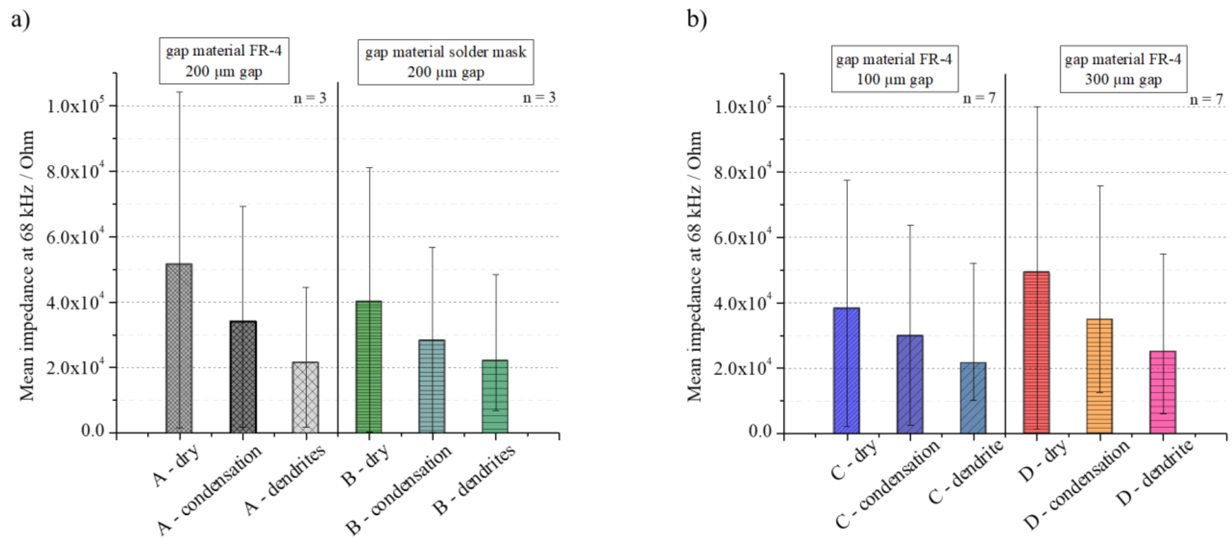


Figure 7.8: Mean impedance at 68 kHz values for each of the conducted experiment series A-D. Values are given for "dry" board state (before cooling profile was initiated), as well as "condensation" state (conterminous with leakage currents exceeding 1 x 10^{-4} mA in the next sequence) and "dendrites" state (state conterminous with leakage currents exceeding 1 x 10^{-2} mA in the next sequence). Error bars represent minima and maxima values of three measurements (left graph), respectively seven measurements (right graph).

For 100 µm gap Cu test structures on FR-4 base material (series C, blue tilted-striped), the mean dry surface impedance of 3.8 x 10^4 Ohm is reduced to 3.0 x 10^4 Ohm before "condensation" current is reached upon DC application. Prior to formation of dendrites, an impedance in average of 2.2 x 10^4 Ohm describes the water film. If the Cu-Cu distance amounts to 300 µm (series D, red cross-striped), the mean impedance in dry state is 4.9 x 10^4 Ohm. Over the course of condensation, it drops to 3.5 x 10^4 Ohm and reaches 2.5 x 10^4 Ohm right before dendrites can bridge the gap. Overall, for all the series, irrespective of the cooling rate and time to gradual formation of the water layer, transition of transient water film characteristic resulting in ECM can be retraced by EIS. The passage into the critical regime can be described by a 68 kHz-impedance value to approximately 2 x 10^4 Ohm. Independent of gap size or substrate material, once this condition is reached, dendrite formation occurred upon application of DC bias for 3 minutes.

D. Gravimetric measurements for approximate quantification of condensed water

Gravimetric measurements were performed for each five measurements in (i) “condensation” region (leakage current exceeding 1 x 10^{-4} mA) and five measurements in (ii) “dendrites” region (leakage current exceeding 1 x 10^{-2} mA). For evaluation, these results were compared with the mean EIS-impedance values at 68 kHz obtained from the preceding EIS-sequence as shown in Figure 7.9 along with minima and maxima error bars. An average of 2.6 mg of water was collected over the comb structure area (5.25 cm^2) in the “condensation” region. The related mean impedance value is 3.5 x 10^4 Ohm. Figure 7.9a) shows the typical surface view of the comb structure under this condition. Visible droplets have formed on the Cu-tracks as well as between the gaps. The largest droplet in the observed area is expanded to 190 µm. However, total bridging of the water layer across the gap at this point is not apparent. In the “dendrites” region, the mean measured amount of water on the comb pattern is 6.0 mg. The impedance value measured under this condition has dropped to the mentioned·10^4 Ohm-region. Typical surface view in Figure 7.9c) also shows that the overall amount of condensed water has increased compared to the “condensation” region. The Cu-traces are almost fully covered and the droplets have merged and grown significantly. The gaps are bridged at distinct points (marked by white arrows). The picture was taken with a monochrome filter to enhance the visibility of droplet edges.

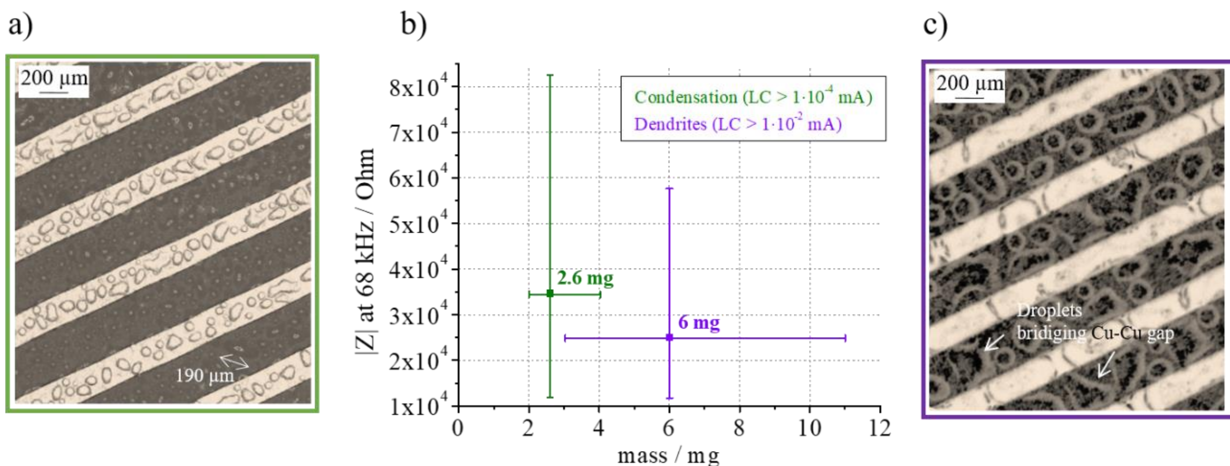


Figure 7.9: a) and c): Microscope images show the surface right before mass measurement for “condensation” region (a) and “dendrites” condition (c, image obtained with monochrome filter for better visibility of droplet boundaries). b) Impedance at 68 kHz frequency and mass obtained from each five gravimetric measurements in transition area and ECM area. Values represent an average with deviation bars minima and maxima.

IV. DISCUSSION

The formation of a very thin water layer on a PCB surface under transient climate conditions causes numerous reliability issues, one of the most prominent ones being ECM. Variations in humidity and temperature of the external climate affect temperature and humidity inside the enclosure of an electronic system (such as on the surface of a PCB). This can result in transient condensation, sometimes only lasting a few minutes. However, these events can still cause significant damage, as a water film can result leak current and ECM. Material and design parameters of the boards strongly influence the water film buildup, especially the transition steps in dew formation, merging of droplets, and development of a continuous layer. For understanding the failure occurrence, the water film buildup that leads to ECM should be understood. Commonly used test methods are based on DC voltage application and leakage current measurement, which is not only destructive due to DC voltage application, but also provides little information on progressive water film buildup. The results presented in the paper show that the EIS method can be used instead for tracing the progressive water film buildup to the critical level required, instead of waiting for the actual failure as with the DC method. The advantage is that the EIS is non-destructive and therefore allows repeated testing. The time of testing could also be reduced, as there is no need to wait for the statistical occurrence of the DC failure. By combining the two types of measurement in an alternating manner in this work, the results show that the course of water layer formation until bridging of a Cu-Cu gap and providing a pathway for dendrite formation can be clearly traced by EIS.

In order to assess the likelihood of migration by means of EIS with progressive water film buildup, it is important to analyze various parameters for their suitability in predicting water film formation. Previous work in this field has already shown that the impedance at frequencies in the 10 kHz region is suitable to measure increased on water load on PCB patterns [22]. The broader spectra measured in this work (exemplarily shown in the Bode Plot in Figure 7.5) confirm these findings. In this paper, the values at 68 kHz frequency were used for evaluation, as both impedance and in phase shift clearly detect all stages of condensation from droplet formation until bridging of the gap. Additionally, it contained the smallest noise in dry state, hence displaying a clear transition into wet state. However, the results also confirm that in general all frequencies in the domain ≥ 10 kHz and ≤ 100 kHz can be used for an approximation of the condensation (Figure 7.5). Related work has also shown that the effect of water film formation is not limited to this frequency range. Condensation experiments with similar PCB-patterns have shown the effect of water bridge closing is evident also for frequencies down to 1 kHz [31]. Even though the condensation detection is not constraint to the high frequency range, the fast transitions of the provoked dewing process require a fast real-time measurement. For the test case, is therefore

appropriate to limit EIS scan times by avoiding lower frequency region. This way, considerable changes in water film status during a single scan are prevented, which improves interpretation of the results.

Overall the results in Figure 7.6 and Figure 7.7 show that the EIS signal can predict the gradual water film buildup, and conditions at which application of DC cause electrochemical failure. If this test is carried out without DC bias, the EIS result corresponding to an interval between 65 – 75 minutes could predict the possibility of ECM failure under DC condition, however without damaging the test PCB as in the cases of DC testing. This way, EIS can be used for checking different PCB design and layouts for their propensity for leakage current and ECM under possible transient condensing conditions. The robustness of designs could be benchmarked in this manner at different stages of an electronics development process.

The condensation test results for the test structure A-D in this study show that impedance and leakage current progression can be generalized as depicted in Figure 7.10. The intersecting point between the impedance and leak current shows the transition area where the leak current suddenly increases due to dendrite shorting, while the impedance drastically decreases. Prior to this, the impedance value shows a gradual decrease with progressive condensation, while the leak current shows a more steady range. Overall, these features are evident on all the plots in Figure 7.7. This indicates a general trend for water film buildup and transition to failure, irrespective of the gap size and nature of the surface. The only difference between the gap size and surface characteristics are on the time for the transition period. Larger gaps exhibited longer periods. This impact of gap size on the time to bridge can be seen when comparing series C and D. Structures in series C have a smaller gap size compared to D (100 µm vs. 300 µm). So even though the applied electrical field is the same, the transition period for 300 µm gap is extended up to twice as long as compared to the values for 100 µm gap.

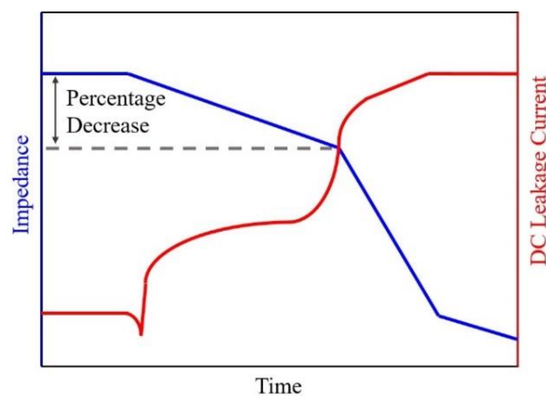


Figure 7.10: Schematic representation of EIS-impedance and DC leakage current progression during condensation from dry state until pronounced dendrite formation.

The impact of surface nature in time for water bridging and ECM has also been shown in literature. It has been elaborated for FR-4 and Polyimide substrates that differences in surface roughness and heat conductivity result in different condensation scenarios [32]. Another study elaborating the time to form a water bridge on a rough and a smooth solder mask finish showed that bridges tend to form faster on rough surfaces. This was due to the fact that for smoother surfaces, the condensed water forms concentric droplets, while irregularities of rough surfaces enhance droplet merging and buildup of a film [33]. Comparing with the specimens in this study, samples with FR-4 laminate surface have higher roughness than solder mask. The results confirm faster time to dendrite for the rough FR-4 laminate compared to solder mask surface (55 minutes vs. 60 minutes, Figure 7.7a) and b)). From the results in Figure 7.8, it can be obtained that by the use of EIS, the ECM-critical status for both surfaces can be assessed, even though they vary in their character. An ECM-critical water film is reflected generally for both by 2.2×10^4 Ohm.

The additional gravimetric measurements complement the electrochemical measurement results and surface micrographs. The average water amount measured across the whole test structure roughly doubles from the point of first detection of condensation until the formation of closed dendrites. The mean impedances calculated for “condensation” and “dendrites” (Figure 7.9) show a significant reduction, hence larger amount of condensate between these stages. When looking at the pictures (Figure 7.9a) and c)) it is apparent, that the statement on a water layer thickness is arguable, as no uniform water layer is established. Instead, there are spots of higher and lower thickness. Even though the water film in the first stages of condensation cannot be considered evenly distributed, the values give a good representation of the transition states the system is passing through before ECM is enabled. The water layer “thickness” in the “condensation” regime is 4.97 µm. In the “dendrites” regime it has more than doubled with a value of 11.46 µm. Previous work in this area has shown that a water film thickness that is considered as “bulk water” amounts to a thickness of 6-40 µm [34]. The lower value domain is found in between the two states determined in this work, indicating that migration in the tested condensation scenarios is associated with the beginning of the “bulk water” status. EIS has shown to be able to distinguish the passage into this area by an impedance reduction.

In order to exploit all of EIS efficiency, the possibility of electrical equivalent circuit fitting can also be considered. This can serve the purpose of understanding the processes in more detail. In addition, various EIS-parameters can be evaluated in their strength to retrace water film buildup prior to dendrite formation. For the sample setup in this work, different equivalent circuits could be used to describe the system. Two potential ones are shown in Figure 7.11. Equivalent Circuit 1 (Figure 7.11a)) is a parallel circuit of resistor *R* and capacitor *C*. In the dry state, both components describe the characteristics of the substrate. For fitting of the data in condensed state, the same circuit can be used to represent water adsorption to the substrate

and changing characteristics of C and R. Hence, the two variables obtain different values, depending on the system status based on water bridge buildup. In an alternative approach, also a more elaborate circuit could be used (Figure 7.11b)). Equivalent Circuit 2 is comprised of a capacitor ($C_{water\ layer}$), describing the capacitance of the bulk with absorbed water. $R_{water\ layer}$ epitomizes resistance of the bulk and condensate. $Q_{double\ layer}$ represents the imperfect double layer capacitance at the electrode/water interface. It is assessed by the parameter a, obtaining values between 0 and 1. $a = 1$ signifies ideal capacitor behavior, $a = 0$ ideal resistive behavior. $R_{charge\ transfer}$ describes the charge transfer resistance at electrode-water interface.

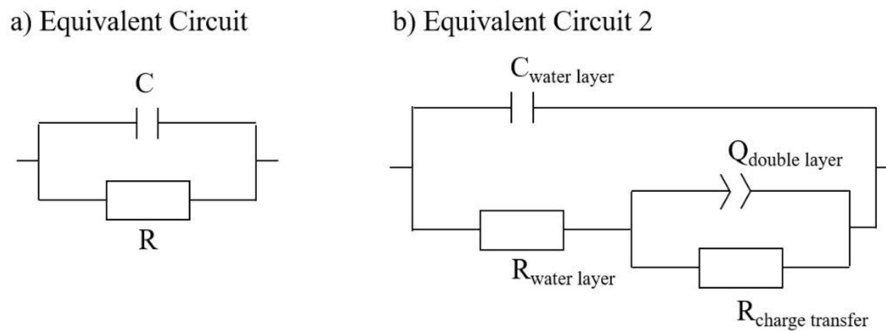


Figure 7.11: Electrical equivalent circuits used for fitting the obtained EIS-data.

By means of EC-Lab® software (V11.20, BioLogic Science Instruments) fitting was exemplarily performed on data of experiment series A. Results are shown in Table 7-2. For the fitting in dry regime, the RC-parallel Circuit 1 was used. For the status of a condensed water layer right before dendrite growth upon DC, both the simple RC-Circuit 1 as well as the more detailed Circuit 2 were used.

Table 7-2: Fitting on EIS data from test A2 (200 µm gap, FR-4) on the basis of Equivalent Circuit 1 for "dry" and "dendrites" status, as well as Equivalent Circuit 2 for "dendrites" status. Parameter values are given with standard deviation.

	"dry" (before initiation of cooling)	**"dendrites"** (before leakage current exceeds 1×10^{-2} mA)
Circuit 1		
C in F	$48 \times 10^{-12} \pm 0.341 \times 10^{-15}$	$109 \times 10^{-12} \pm 0.569 \times 10^{-15}$
R in Ohm	$24.11 \times 10^{6} \pm .015 \times 10^{6}$	$0.126 \times 10^{6} \pm 2.5 \times 10^{0}$
Circuit 2		
$C_{water\ layer}$ in F	-	$60 \times 10^{-12} \pm 1.7 \times 10^{-12}$
$R_{water\ layer}$ in Ohm	-	$5.152 \times 10^{3} \pm 0.160 \times 10^{3}$
$R_{charge\ transfer}$ in Ohm	-	$217.402 \times 10^{6} \pm 0.135 \times 10^{3}$
$a_{double\ layer}$	-	0.767 +/- 0.51

Fitting with Circuit 1 shows that the capacitance value has more than doubled from dry status until condensation allows the formation of the dendrites. The condensation is also displayed in a significant decrease of resistance from approx. 24 x 10^6 Ohm to 0.126 x 10^6 Ohm. The parameter obtained from Circuit 2, involving a more detailed description of the system under condensation regime; show a capacitance in the same value range as also for Circuit 1 (10^{-12} F region). The resistance $R_{water\ layer}$ is only in the 10^3 region, indicating the condensate present all over the surface. Still the charge transfer resistance is in the 10^6 Ohm level. The parameter $a_{double\ layer}$, describing the character of the constant phase element is within a value of 0.767 in the capacitive region. However, the standard deviation is considerably large, so also a considerable resistive character cannot be ruled out from the fitting results.

Generally, the equivalent circuit modelling for the data in this work needs to be considered with caution for two reasons: (i) the limited frequency range, as well as limited number of measurement points within that range hamper the goodness-of-fit. A broader range and more measurement points would deliver more reliable results. (ii) The use of equivalent circuit elements like the CPE further worsens the general problem of ambiguity of fitting data to equivalent circuits. With two parameters of that element that are adaptable to the data, the transferability to real-life processes is not clearly allocated.

Still, fundamentally, the possibilities to model EIS data with real-life equivalents is of great benefit when employing the method. Changes in resistive and capacitive circuit parameters give an overall impression on the proceeding water film formation. Testing scenarios that involve slower condensation or long-time near condensing conditions would generally allow longer scan times, thus broader frequency ranges. In this area, fitting can be useful. The experiment scenario in this work is primarily described by the capacitive response of the EIS method, especially in the used frequency range. The surface prior to cooling is considered dry, and it can be regarded as two Cu-plates, separated by a dielectric of laminate and air. This results in a high equivalent resistance and low equivalent capacitance in the case of EIS measurements. With regard to DC signal application, this is mirrored in a low value for leakage current. The EIS data is governed primarily by the epoxy-based laminate, as the dielectric constant is larger than that of air (ε_{air} = 1.00053, ε_{epoxy} = 2.8-4.6) [35]. With commencing condensation, droplets start to form on Cu tracks and on the PCB laminate in the gap. These have an impact on the capacitance, as the permittivity of water (ε_{water} = 79.5) needs to be regarded [35].The contribution of the resistance increases likewise during the process. Also in the case of DC testing, the condensation results in a resistance drop. Once individual droplets across the gap merge into an interconnecting layer, also EIS and DC tests detect this state. As the layer builds up further and the impact of water permittivity increases, this is gradually identified in EIS, up to a point where the signal is only determined by ε_{water}. The DC testing fails to clearly distinguish the water layer growing in height. Once the dendrite has fully closed the gap, the resistive character of the dendrite

governs the system. The sensitivity of EIS towards all the small changes in the test system is an advantage compared to the DC measurements for PCB applications.

Understanding the preconditions that lead to corrosive events is what enables corrosion control. A criticality estimation for electronics can be made at an early stage in development for different geometries, design elements, materials and climatic environments. The fact that EIS is able to detect an ECM-water critical status and thus provides a prediction of DC failures is a major benefit. The method being non-destructive to the specimen, and therefore allowing re-use for various climatic scenarios is valuable for testing.

V. CONCLUSION

1. The data acquisition by sequential EIS and DC measurement permits the assignment of EIS values signifying a water layer pronounced enough to enable ECM. For the samples under tests, it is shown that independent of surface material or CuCu distance, a 68 kHz impedance of approx. 2×10^4 Ohm needs to be considered ECM critical.

2. Gravimetric measurements of average water amount across the area of sample structure indicate that the quantity of water doubles from the point to first detection of condensation in DC measurements until the formation of closed dendrites. ECM in the tested scenarios can be identified with “bulk water” layer thickness. EIS measurements can identify the transition into this region.

3. The results of this work show that the EIS technique can detect an early stage water adsorption as well as following condensation processes. The changes in signal are prominent before dendrite shorting occurs. Accordingly, the method allows to determine criticality for ECM and other humidity related processes non-destructively. In this manner, a reliability prediction for various different design elements and materials can be facilitated.

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8. NON-DESTRUCTIVE ELECTRICAL APPROACHES TO LOCALIZE CONDENSATION EVENTS ON PCBS

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Simeon Lange, Yannis Grau

Abstract – In reliability assessment of electronics, humidity induced failures are a prominent concern. In the automotive electronics sector, the main component Printed Circuit Board Assembly (PCBA) is exposed to various temperature and humidity conditions, often rapidly changing. This can lead to local condensate formation on the PCBA surface. In case of a water bridge formation between oppositely biased metal tracks or pads, this can result in electrochemical migration, at its worst in dendrite formation, resulting in a short circuit. Detailed knowledge on the conditions for this failure mode is essential in electronics development. This work focusses on the determination of localized condensation events on PCB surfaces. Two approaches are followed to evaluate the occurrence of condensate and the influencing parameters. Firstly, AC impedance spectroscopy was used to obtain the humidity profile on a PCB surface with a number of interdigitated patterns around a heat-generating component to assess the relation of PCB self-heating and condensation. Measurements were performed on copper comb patterns with 100 µm width. Impedance data of the structures was used to map the relative effect of humidity on patterns located at different distances from the heating component. In a second approach, Time Domain Reflectometry (TDR) was used to locate the water droplets on a PCB surface with solder mask covered copper traces. TDR was also employed to evaluate the impact of flux residues on condensation. A more severe condensate buildup at flux residue spots compared with a clean board was determined.

Keywords – AC impedance spectroscopy; time domain reflectometry; water film formation; electronic reliability; humidity; corrosion

I. INTRODUCTION

Long-term stability of electronics is a major concern for various device categories. Particularly in the field of automotive electronics, lifetimes of 20 years or more are typical requirements. For years, it has been a focus to improve the reliability of electronic devices [1]. Specially developed evaluation criteria for durability are defined in standard testing procedures. Reflow soldered setups for automotive electronics are tested according to JEDEC J-STD 020, including quality assurance for different climatic environments [2]. One key aspect in the reliability of automotive electronics is humidity. The operating conditions of common designs such as control units impose high demands. The electronics experience extreme temperature and humidity in the field [3]. The climatic conditions of the devices, for example due to day and night shifts, cause humidity buildup inside the enclosure, sometimes resulting in transient condensation. Due to these

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transient events, potentially even thin films of dew can form on boards [4,5]. The high humidity ambient is prone to provoke corrosive processes of the electronics, which can lead to a malfunction of the devices [6]. One of the main corrosion failure causes is electrochemical migration (ECM) on Printed Circuit Board Assemblies (PCBAs), which is the main component of most electronic devices. ECM takes place when two oppositely biased electrodes (for example solder pads or component legs) are connected via an electrolyte layer. If a potential bias is applied, metal ions at the anode are created by oxidation. Under the applied potential, they move through the electrolyte towards the cathode, where they are reduced in the form of a dendrite growing towards the anode. If this process is sustained long enough, the filament forming between anode and cathode can create an electrical short leading to an electrical failure [7,8]. Multiple materials on a PCB used for automotive electronics are affected by potential ECM development. Among them are tin, silver, and also intermetallic phases like in solder joints composed of Sn/Pb/Ag, Sn/Ag/Cu or Sn/Zn/Bi with different migration elements [8–11]. The short circuit is often intermittent, because the dendrites easily burn when high currents pass through them once the water bridges evaporate [8]. Thus, an assessment of criticality for specific design elements and humidity environments is even more difficult, as the establishment of a root-cause relationship after testing is hampered.

Water film formation on the PCB surface is the prerequisite for the failures to occur. Accordingly, PCBA setups are designed to minimize the risk of condensation. In development, special attention is given to suitable placement of actively powered components on the PCBA product. Another key factor is the implementation of reliable manufacturing processes, using adequate materials and avoiding contamination. Both of these factors incorporate two of the most important elements that govern water film formation on a PCB surface: (i) surface temperature distribution and (ii) presence of contaminants. The surface temperature aspect of a PCBA is greatly governed by the self-heating due to heat generated by the components and its effect on humidity related problems. Self-heating of the PCBA under on-conditions of the device can prevent condensate formation to a certain degree. However, the absolute humidity within the system remains similar. Thus, the effect is the displacement of the humidity from hot to cold PCB areas. Therefore, under self-heating conditions, distribution of the heat on the PCB is a crucial factor. A heat-generating component on the surface can be effectively used as a mean to control humidity effects. By proper component placement, the distribution of heat removes high humidity from critical areas. The stronger the heat radiation of a powered component, the larger is the PCB surface temperature in the surrounding. Consequently, the likelihood of condensate formation in the vicinity is lowered. Investigations on standard biased PCBAs (non-hermetically sealed) showed that temperatures of 50 °C are reached locally. Water spray tests confirmed evaporation within minutes in those regions [12]. In PCBA layout development, the knowledge on the impact of heat radiating components is therefore crucial to produce reliable designs.

Surface impurities, particularly when of ionic character, are another key factor in terms of condensation formation on a PCB. Impurities that tend to interact with moisture, such as dust, significantly contribute to water film formation [13]. In addition, manufacturing process related contaminants can be problematic. Especially acids from solder flux residues are considered critical. The enhancement of corrosive processes is thereby affected in two ways: firstly, the hygroscopicity of the compounds promotes condensation already at low relative humidity levels [14]. Secondly, the dissolving of ionic contaminants into the condensate film increases its conductivity and corrosion reactions can speed up [15].

Conventional methods to assess the humidity reliability of PCBAs are based on direct current (DC) testing. Particularly common is the so-called SIR (surface insulation resistance) test [16]. It measures the resistance across the surface between electrodes on a PCB under humid conditions. In test scenarios, interdigitated comb patterns are used in many cases. The respective SIR value detects potential leak current routes along the surface or through near-surface interior of the substrate [17]. The test is conducted in different climatic scenarios (for example 1000 hours at 40 °C and 92 %rH) as well as for different voltage classes, ranging from 5 V up to 1250 V for high voltage applications such as e-mobility [18].

A drawback of the SIR method is not only that the dendrite-provoking DC voltage is destructive to the sample, but the electrochemical polarization of the involved anode and cathode at the high bias potential impedes an understanding of the initial water film buildup characteristics and ECM formation [19]. In order to comprehend the robustness of the system during testing, it is preferable to achieve an early detection of potential failure modes. Hence, the detection of the water bridge buildup itself would be beneficial for predictive assessment corrosion criticality. The formation of a water bridge starts with the initiation of condensation. An initial nucleation of water droplets on the substrate occurs if water vapor is governed by a pressure larger than its saturation pressure, resulting in a transformation into liquid to minimize energy. The isolated dew droplets grow until they touch at their perimeters and start merging. The process can continue until a distinct surface area is fully covered [20,21]. In this manner, the condensate formation relates to the buildup of a closed water bridge between metal electrodes, providing a pathway for ECM [22].

In order to detect condensation as initial boundary condition for ECM, methods based on alternating current (AC) or low voltage pulses at high frequencies can be employed. AC impedance spectroscopy is a technique that is based on the application of an alternating voltage with a low amplitude [23]. If the potential is not limited to one frequency, but a frequency range is covered, the method is referred to as Electrochemical Impedance Spectroscopy (EIS) [24]. The small perturbation is not harmful to the sample and the response at a distinct frequency allows detailed characterization of the resistive and capacitive properties of the system [24,25]. In relation to corrosion assessment, respectively the formation of water layers, impedance

spectroscopy has been used in various contexts. Among them are atmospheric corrosion of electronic components under thin electrolyte layers or corrosion monitoring of engineering materials such as steel [26,27]. Furthermore, it has been used to assess the corrosiveness of different condensation enhancing fluxes or to assess flux residue interaction with water vapor by detecting an impedance decrease resulting from the water layer formation between contacting lines [19,28].

Another possible method that can be used for detection of humidity is Time Domain Reflectometry (TDR). The technique was originally developed to localize mechanical defects in electrical wires [29]. It is based on the application of an incident picosecond length pulse in the mV range into electrical conductor lines. If an interface with a different characteristic impedance is present along the line, this will cause the incident signal energy to be reflected back to the source. The reflected signal correspondingly is a function of transmission line characteristics and the characteristic impedance of the interface. The travel time of the signal can be associated with the actual mechanical length of a specimen, allowing a localized impedance profile [29]. The signal propagation, hence the impedance progression, is determined by the dielectric properties of the media surrounding the transmission lines. Utilizing this, TDR has also been used to determine the water content of porous media like soil or for determining the water amount in fuel tanks [30–32]. In the context of PCBA reliability, TDR is used to indicate discontinuities in electrical paths and to ensure impedance-control for base laminates [33]. Impedance controlled PCBs are becoming highly relevant, as the high-frequency transmission range is used in more and more devices. It is therefore needed to ensure that the changing dielectric properties of a laminate in high humidity ambient or other stress environment do not interfere with signal propagation. However, there is no reported information in the literature on the use of the TDR technique for detecting the humidity related condensation formation in connection with electronics.

The present paper focuses on the understanding of water level buildup on a PCBA and its measurement by EIS and TDR. In the first part of this work, impedance spectroscopy was used to assess the impact of surface temperature on water layer buildup. In order to comprehend the self-heating effect, a powered board has been replicated by mounting a heat-radiating diode on a board equipped with measurement structures. Repeated condensation was provoked on the test board by temperature cycling. At distinct distances to the diode, impedance was measured and related to the severity of condensation. In the second part, the localization of water droplets via TDR measurement was shown for two different droplet volumes. TDR measurements were also used to verify the condensation enhancing impact of flux residues. For this purpose, a contaminated board was compared with a bare board during a cyclic condensation scenario.

II. MATERIALS AND METHODS

A. AC impedance measurements to assess humidity effects under self-heating conditions on a PCB

A.1 Special test board with heating element and multiple SIR comb patterns for condensation testing

Figure 8.1 shows a schematic of the test board constructed for testing the humidity effects under self-heat conditions using AC impedance measurement. The board consists of a matrix composed of 54 Cu comb patterns with each pattern having a size of 3 mm x 3 mm dimensions at distances of 0.7 mm. The copper width was 200 µm, the Cu-Cu gap at the interdigital regions was 100 µm. Base material for the PCB was standard FR-4 laminate. As shown in Figure 8.1 an SMT diode was mounted in the middle of the comb matrix on the PCB using heat conducting tape. The diode was powered by an external power supply in order to build up a heat profile on the test board. Measurement runs were performed with 0.4 A diode current as a standard. An additional measurement was conducted with 0.2 A diode current to evaluate the impact of a lower heat generation on the condensation process.

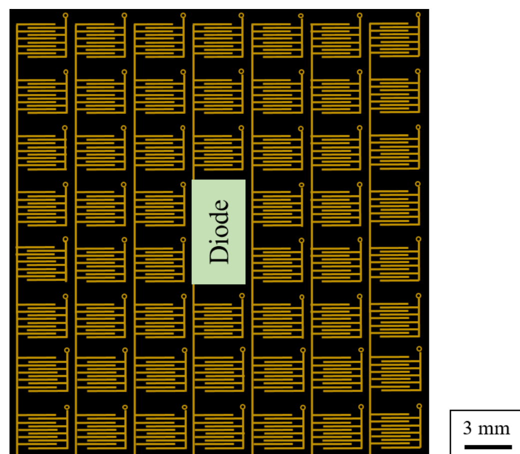

Figure 8.1: Schematic of test board layout with 54 comb patterns and the diode put in the center.

A.2 Climatic Testing

The measurements were conducted in a “VCL4010” environmental test chamber (Vötsch). To provoke condensation on the surface of the board, a cyclic temperature profile at a relative humidity of 92 %rH was applied (Figure 8.2). By fast temperature increase of the ambient climate and due to the time delay in temperature equilibration of the test board, condensation is provoked on the surface. At test start, the chamber temperature was kept at a constant 25 °C for one hour to give time for equilibration. In the first temperature peak, temperature was increased to 35 °C within one hour. The cool down time back to 25 °C was 45 minutes. In the second peak, ramp up from 25 °C to 40 °C was performed within an interval of one

hour. The respective higher heating rate was to ensure a stronger humidity buildup on the surface of the PCB during the second peak. Ramp down time was again 45 minutes. In order to enhance condensation on the heated test PCB, it was mounted on an aluminum plate as thermal mass. A high-resolution imaging camera (AM4115ZTL, Dino-Lite) was installed in the chamber during one of the test runs to obtain in-situ images of the condensation status on the comb structures during the experiment.

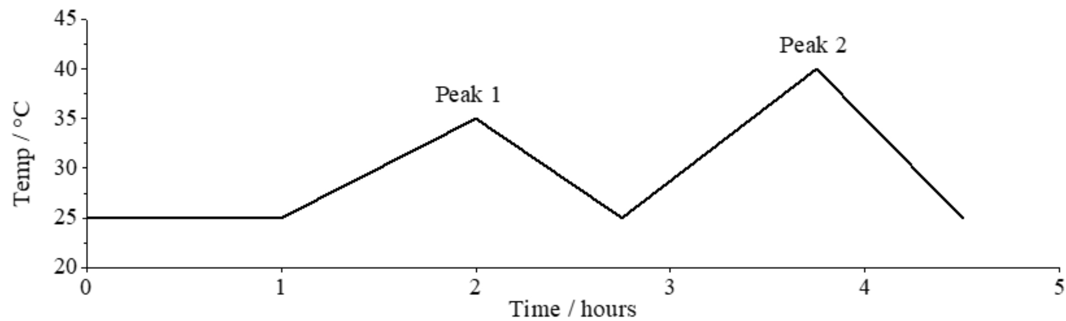

Figure 8.2: Temperature profile performed in climatic chamber at 92 %rH to provoke cyclic condensation and evaporation on the surface of the test board.

A.3 Electrochemical Setup

In order to understand the effect of humidity on the different comb patterns on the PCB, their impedance was measured during the climatic testing. The AC impedance technique was used with an in-house built potentiostat system that provided a signal amplitude of 3 V at a frequency of 10 kHz. The impedance for all of the 54 single comb patterns was measured over time. As the values were obtained successively in matrix mode, for each pattern, the impedance was recorded at every 13 seconds.

B. Time Domain Reflectometry to determine localized condensation

B.1 Electrical measurement setup

For TDR measurements, a Controlled Impedance Test System (CITS 880s, Polar Instruments) was used to send an electromagnetic pulse into the test pattern and detect impedance changes caused by different dielectric properties across the length of the pattern. The differential variant of the measurement was used, meaning the signal was guided through two parallel lines. The signal amplitude was set to 300 mV and the rise time was ≤ 200 ps. The test patterns used for measurement were two parallel Cu traces for differential pair measurements. These were inner-layer tracks, hence covered with a solder mask layer. Electrical contact of test boards to the measuring device was made using coaxial cables attached to soldered SMA-connectors.

B.2 Testing scenarios used for TDR measurements

B.2.a Location and volume of water droplets

TDR was used to evaluate the possibility of determining the location and relative volume of water droplets on the surface of the test boards. For this purpose, two parallel Cu traces with a length of 120 mm were used for measuring. To compare detectability of droplet volume, two droplets with each 10 µl DI-water (Figure 8.3a)) were pipetted onto a board. On the second board, two droplets with each 30 µl DI-water were dispensed (Figure 8.3b)). The droplets were each placed at 60 mm and 105 mm distance from the SMA-connectors. To avoid external influences like shaking or strong air circulation, the boards were placed in a switched-off climatic chamber (SH-242, Espec) for TDR measurements.

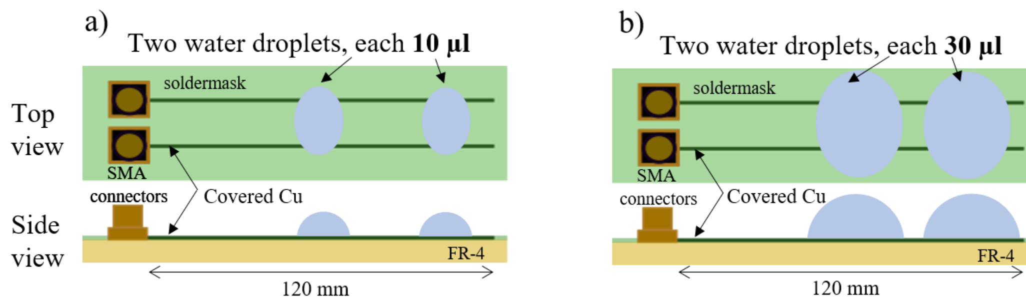

Figure 8.3: Schematic top and side view representation of sample with solder mask covered Cu traces on FR-4 laminate and two droplets of 10 µl (a) and 30 µl (b) water pipetted on 60 mm and 105 mm distance to SMA connectors. Dimensions are not to scale.

B.2.b Impact of flux residue on localized condensation

In order to determine the impact of flux residue on the severity of condensation and simultaneously obtain a local profile of condensate formation, TDR measurements were conducted on a bare board (Figure 8.4a)) as well as a flux-contaminated board (Figure 8.4b)). Like in the water droplet tests, a board with structures of each two Cu traces for differential pair measurements were used, though Cu-length was 90 mm. The flux used was a commercially available automotive flux for selective soldering. After dispensing approx. 5 µl on the Cu traces at a length of 40 mm from the connectors on the test board, it was heated up to 100 °C for five minutes, representing the state of not fully cured flux residues after a selective soldering process. This means that the temperature reached is 140 °C below the intended temperature of 240 °C at the solder joint during soldering.

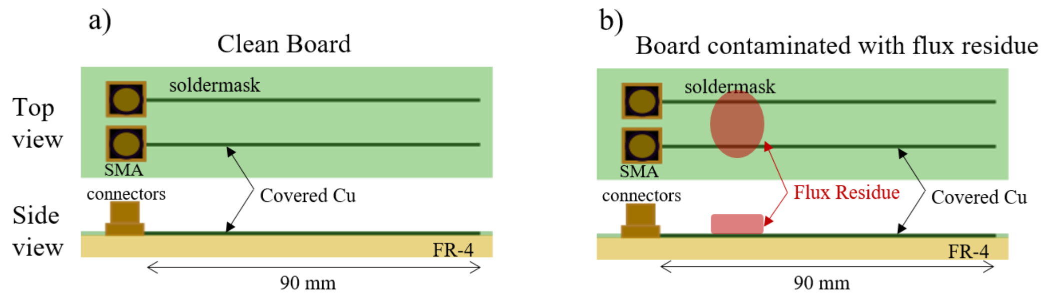

Figure 8.4: Schematic top and side view representation of sample with solder mask covered Cu traces on FR-4 laminate for bare board reference (a) and board contaminated with flux residue at approx. 40 mm distance to SMA connectors (b).

To provoke repeated condensation and evaporation on the surface of the boards, a cyclic temperature profile was imposed on the samples in a climatic chamber (SH-242, Espec). Initially, the relative humidity was set to 97 %rH for 250 minutes (Figure 8.5). Temperature was ramped up first to 50 °C within an interval of 60 minutes and ramped down in the same interval. In a second ramp, 55 °C were reached within 60 minutes and temperature was cooled down back to 25 °C within another 60 minutes. Stronger temperature increase for the same time in the second peak was supposed to result in somewhat stronger condensation compared to first peak. At the end of test, the humidity in the chamber was ramped down to 50 %rH over the course of 60 minutes. During the climatic profile, measurements of mean impedance for both test boards were activated manually. In addition, for the flux-contaminated board, localized impedance spectra related to Cu-length were obtained periodically.

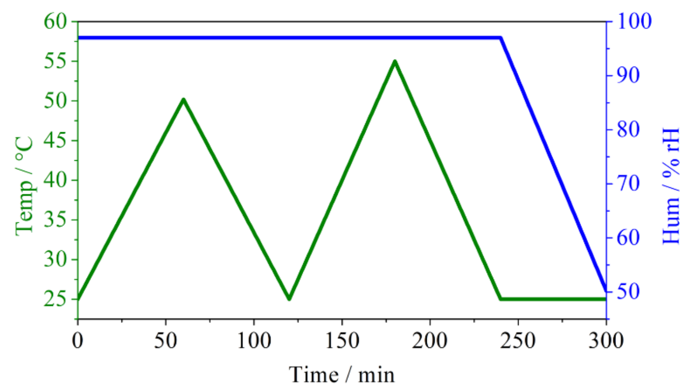

Figure 8.5: Climatic profile imposed on bare test board and contaminated test board while performing TDR measurements.

III. RESULTS

A. AC impedance measurements to assess humidity effects under self-heating conditions on a PCB

A.1 Directional progression of impedance during condensation and evaporation with respect to distance from heating component

To assess the impact of distance to the heat radiating diode, the impedance values over the course of the climatic profile were evaluated directionally with increasing distance to diode (see Figure 8.6 for comb pattern numbering for future reference). The patterns in the top left (blue), top right (orange) and bottom left (green) corner were used for evaluation. Three comb structures in the bottom right corner of the diode showed a malfunction, presumably due to loss of wire connection to the test system. Therefore, this area is was not included in the evaluation.

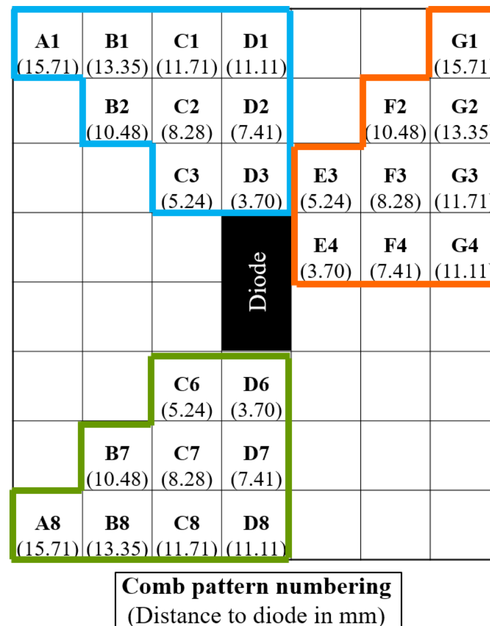

Figure 8.6: Numbering of comb patterns used for evaluation. Number in brackets for each pattern shows the distance of the comb center to the middle the diode in mm.

The heat impact that the powered diode signified for the board surface was assessed with temperature sensors in an additional measurement during the climatic profile shown in Figure 8.5. Figure 8.7 shows the temperature values for the moment right at the start of testing and just seconds after the diode was turned on (a) and the values at the maximum of temperature peak 1 (b). The results demonstrate a slightly non-homogenous temperature distribution on the board surface. This is due to the airflow in the climatic chamber, which causes directionality in the heat distribution. The data of peak 1 reveals a considerable

temperature difference for the top, especially top left part of the diode. While patterns B2 and F2 show temperatures of 26.33 °C and 26.63 °C, the bottom structures with the same distance (B7 and F7) are only at 25.86 °C and 25.81 °C. The difference of the two measured structures closest to the diode (C3 and E6) is even more significant. Compared to the start of testing (Figure 8.7a)), E6 has increased from 25.38 °C to 26.63 °C (by 1.25 °C), and C3 even from 25.6 °C to 27.7 °C (by 2 °C).

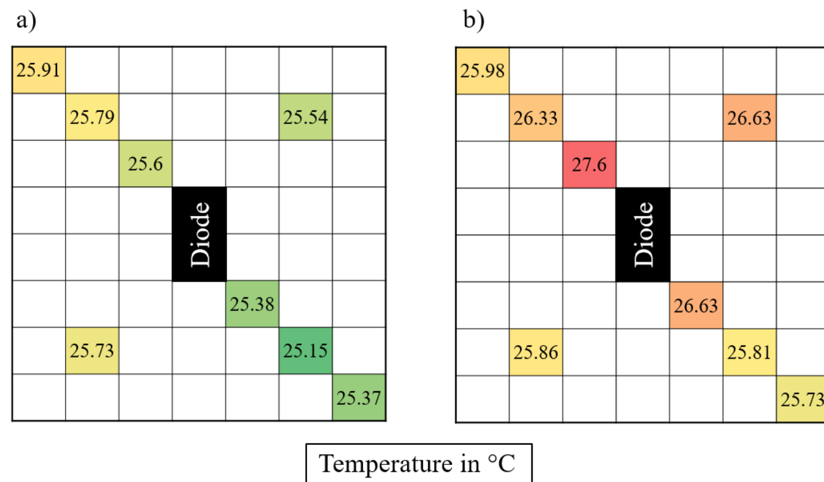

Figure 8.7: Temperature data obtained from measurement on surfaces of selected comb structures. a) Values right before chamber start and just after diode current was applied. b) Values during maximum of peak 1. Coloring indicates highest values in red and lowest values in green.

In order to assess the impact of condensation, the progression of impedance values are shown for each three combs with increasing distance from diode center for three directions: (i) top left (C3, B2 and A1, Figure 8.8), (ii) top right (E3, F2 and G1, Figure 8.9) and (iii) bottom left (C6, B7 and A8, Figure 8.10). For all patterns, an example of the impedance data for the first run (a) and the fourth run (b) of experiment repetition with 0.4 A diode current are shown. Run 2 and 3 are not shown, however they progress similar as the data shown in the presented figures.

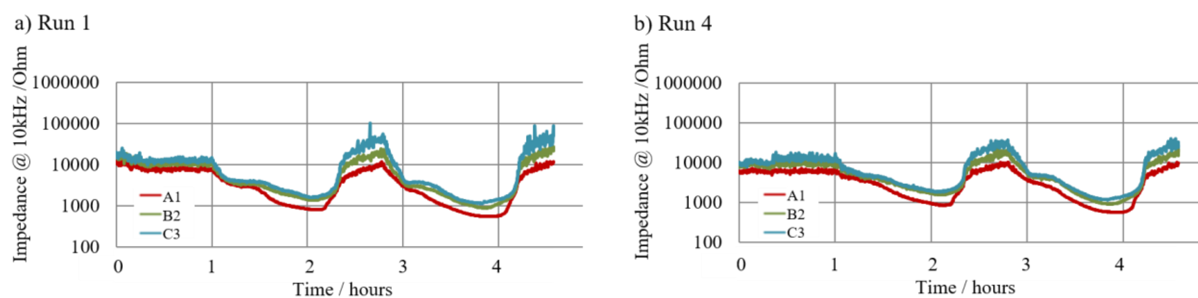

Figure 8.8: Progression of AC impedance values during temperature cycling profile for top left comb structures A1, B2 and C3.

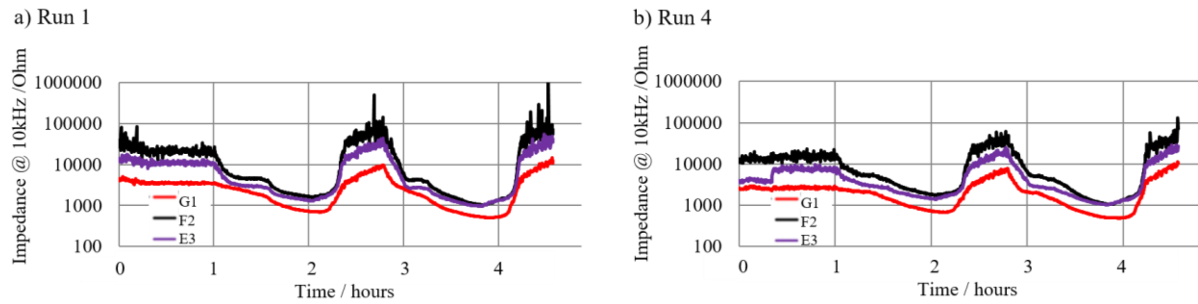

Figure 8.9: Progression of AC impedance values during temperature cycling profile for top right comb structures G1, F2 and E3.

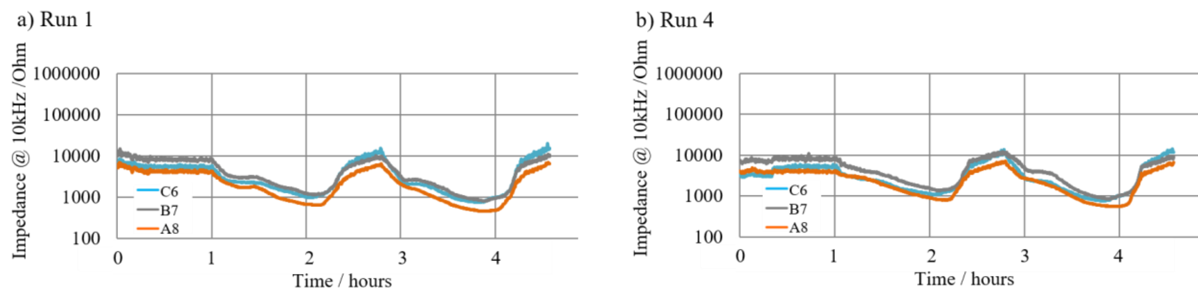

Figure 8.10: Progression of AC impedance values during temperature cycling profile for bottom left comb structures C6, B7 and A8.

Generally, it can be seen from the impedance curves that all of the comb patterns follow the cyclic climatic profile imposed on the board (Figure 8.2). In the first hour of the climatic profile, the temperature is kept at a constant of 25 °C to allow equilibration of the conditions. In this period, the impedance values show a stable range of approx. 10000 Ohm. Individual structures deviate from this range, whereby the largest difference can be seen for the top right comb patterns (Figure 8.9), where F2 shows higher (up to 81620 Ohm) and G1 lower (down to 2875 Ohm in Run 3) impedances. As the first temperature peak is reached, a drop in impedance for all patterns represents the condensation process. The progression shows a slow decline until approx. 1.5 hours and another stronger decline until 2 hours into the profile. Upon temperature ramp down back to 25 °C, the impedance values rise back to initial values or above, indicating evaporation. For the second temperature peak (45 °C), the impedance progression is analogue; however, the impedance drop is more severe than for the first peak, suggesting stronger condensation.

Comparing the data of comb patterns within each of the quadrants (top left, top right, bottom left), it is recognizable that with increasing distance to diode, the impedance values throughout testing are lower. This behavior represents the stronger condensation for more remote structures, as they are not as strongly affected by the heat radiation of the component. This is evident especially after approx. 1.5 hours (during peak 1) and 3.2 hours (during peak 2). After the initial uniform impedance decline for all patterns, structures

farthest away from the diode (A1, G1, A8) exhibits another strong decrease down to approx. 1000 Ohm. The other six structures closer to the diode (B2, C3, F2, E3, C6 and B7) follow with a delay. Also, in contrast to the outermost structures A1, G1 and A8, the minimum impedances of the inner structures do not significantly reduce below 1000 Ohm. The outmost structures show a minimum value range of 500 Ohm in the second temperature peak after approx. 3.5 hours. The saturation character of this value range suggests that the interdigital comb tracks are fully bridged by a water layer during this period. In the evaporation period after both temperature peaks (approx. 2.2 hours and 4 hours), the impedance rise occurs first for the outer structures. With some minutes delay, the structures closer to the diode also show the impedance increase in uniform manner.

In the overall impedance development, for quadrants top left, top right and bottom left, it is conspicuous that there is a directional dependency in values. The top quadrants generally show higher impedance values than the bottom one, also during condensing conditions. This indicates less water accumulation in these regions of the test PCB. Accordingly, the impedance measurement confirms the surface temperature measurements conducted in an additional run with sensors mounted on some comb patterns (Figure 8.7). The non-homogeneous temperature distribution – supposedly attributed to the directional airflow in the climatic chamber – leads to a directed flow of heat.

In order to receive an impression on the heating impact of the diode on the surrounding condensation, an additional experiment run was conducted with 0.2 A diode current, half of the current used for the previous experiments. For the same comb patterns, the impedance progression is shown in Figure 8.11. The effect of less power and thus less heat radiation is recognizable in lower impedance values, particularly for the second temperature peak (around 3.75 hours). In contrast to the 0.4 A diode current test runs, the patterns that are closer to the diode now also drop below 1000 Ohm impedance.

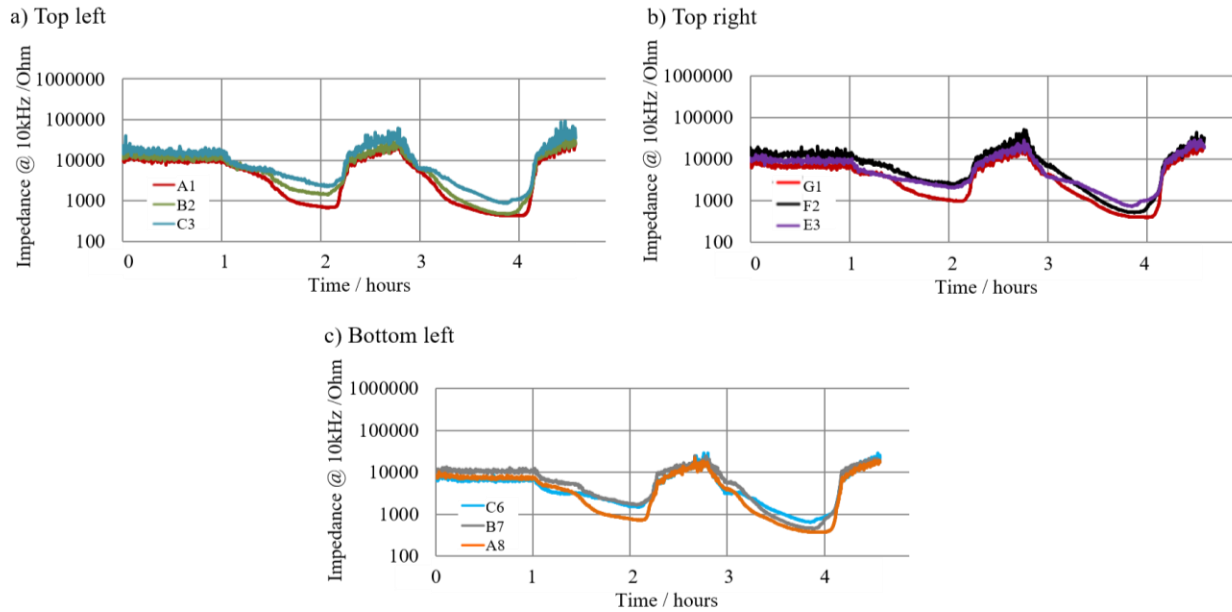

Figure 8.11: Progression of AC impedance values during temperature cycling profile for selected comb patterns of top left (a), top right (b) and bottom left (c) quadrants for 0.2 A diode current.

A.2 Humidity effect mapping across the surface of the PCB based on impedance values

Using the results from the impedance measurements, humidity effect maps of the PCB surface were generated. For this purpose, the typical impedance values corresponding to different levels of water film were assessed from the impedance data. They were correlated with in-situ microscopy images in order to relate the ranges with the establishment of a water bridge between the interdigital traces. Three domains were determined based on this evaluation. These are: (i) impedances > 5000 Ohm for dry board, (ii) impedances between 1000 – 5000 Ohm as intermediate range of condensation, and (iii) impedances < 1000 Ohm for wet range as in formation of water bridges in between the interdigital comb traces.

In order to create a two-dimensional humidity effect map, the logarithmic impedance values for all of the available 51 comb structures were evaluated at certain points in time and classified according to the three impedance domains mentioned above. Figure 8.12 shows the progression of impedances of the patterns corresponding to Run 4 as an example. The color coding was applied on each individual comb structure, indicating (i) dry state in green (Log(imp) > 3.69897), (ii) intermediate state of condensation in yellow (3.69897 ≥ Log(imp) > 3), and (iii) wet state in red (Log(imp) ≤ 3).

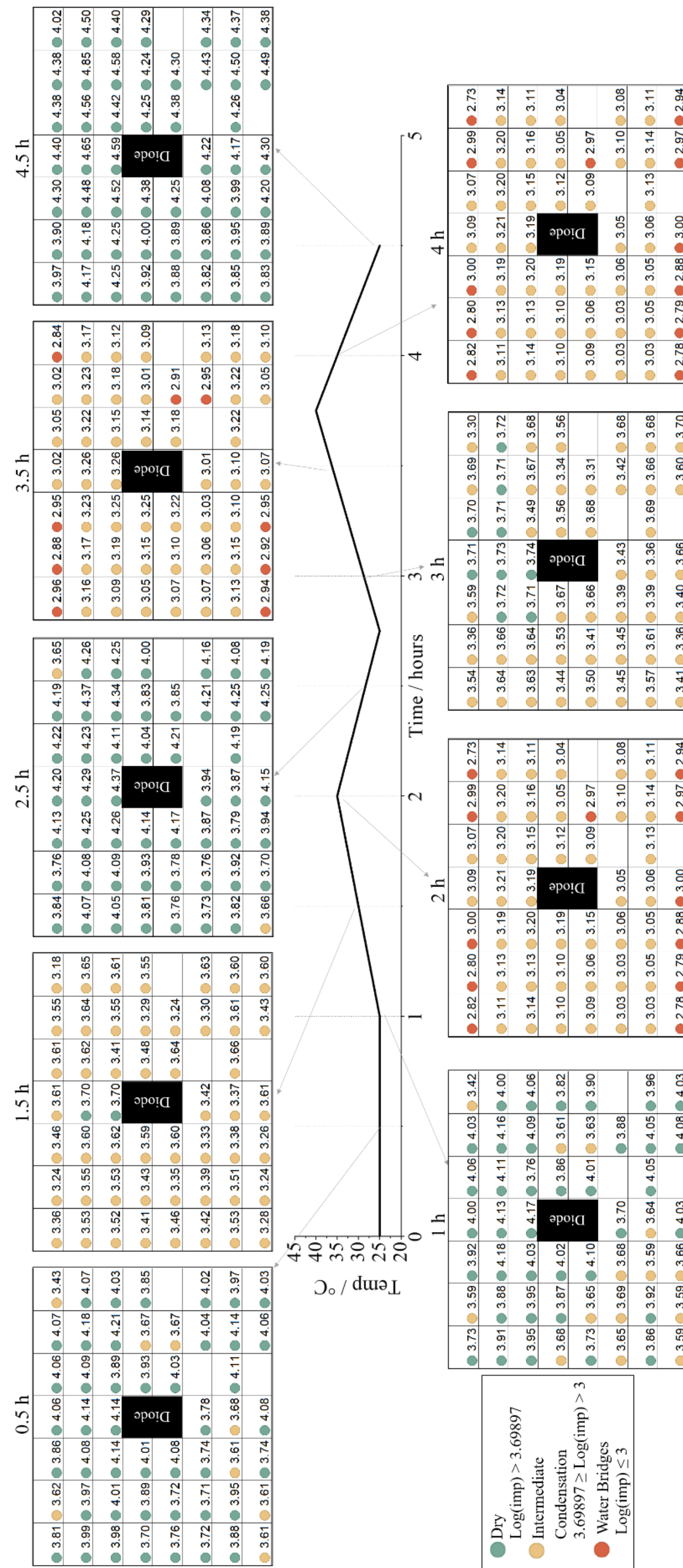

Figure 8.12: Impedance values at distinct points during the climatic profile for all comb patterns of Run 4. Color coding represents humidity status on surface based on impedance classification.

During the equilibration period of 25 °C at 92 %rH, the impedance values after 0.5 hours are predominantly in dry condition (green), with some patterns showing lower impedances values (yellow). These structures with intermediate condensation range continue in this range until 1 hour, with additional patterns in the bottom left corner also reaching this range. After 1.5 hours, all structures show signals corresponding to the intermediate condensation regime, with the exception of two patterns above the diode. At the peak of the first temperature ramp after 2 hours, eleven structures in the outer range as well as structure F5 have fallen below 1000 Ohm (red), indicating water bridge formation. The impedance values of the humidity map obtained after 2.5 hours show that evaporation has proceeded in a way that all patterns attained impedance corresponding to the dry regime (green), with the exception of two outmost structures still indicating slight condensation (yellow). During the second temperature ramp up, the values measured after 3 hours show condensate formation on all structures in the bottom half of the diode and on most of the top half structures. Thirty minutes later, the impedance values show that condensate has formed on all patterns (yellow) and again structures at the outmost area as well as F5 and F6 show water bridges across the electrode gaps (red). Once temperature starts to ramp down again after 4 hours, all patterns still exhibit some form of condensate or even water bridging. At the end of the test (4.5 hours), all patterns have dried (green).

A.3 Assessment of critical water loading related to distance from diode

Based on the information of local condensate formation obtained from the impedance measurement, an assessment of zones with critical water loading can be established for the PCB. A condition that needs to be regarded critical is the formation of a closed water bridge between the interdigital electrodes of the comb patterns. The closed water bridge is the initial requirement for electrochemical migration. Accordingly, the knowledge about up to which distance the diode self-heating prevents condensation that bridges the 100 µm gap allows the assessment of the reliability of the setup.

In order to show this relation, the impedance minima of selected comb patterns for both condensation scenarios (temperature peak 1 and temperature peak 2), were obtained for experiments run 1-4 (all with 0.4 A diode current). Due to the non-uniform heat distribution, the data was again evaluated with directional dependence. The comb patterns used for calculation are highlighted in Figure 8.6 as top left (blue), top right (orange) and bottom left (green). All of the patterns are of a distinct distance to the diode, also listed in Figure 8.6. The mean minimal impedance of all experiment runs for each comb during both condensation scenarios was related to this distance. Figure 8.13 shows these impedance values versus distance of the comb pattern to the diode for the top left (TL, blue), bottom left (BL, green) and top right (TR, orange) quadrants. Based on the impedance values, it is possible to assess less critical to high critical regions around the diode.

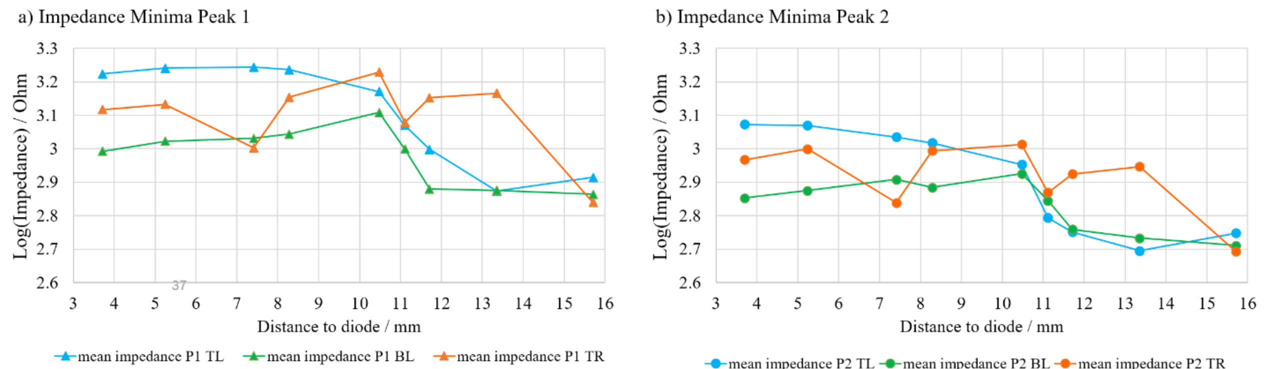

Figure 8.13: Mean impedance values of test runs with 0.4 A diode current related to distance to diode. Curves are shown for maximum condensed state for a) temperature peak 1 and b) temperature peak 2 for top left (TL, blue), bottom left (BL, green) and top right (TR, orange) quadrants.

It is apparent that independent of distance to the diode, the impedances for peak 1 (Figure 8.13a)) lay above impedances of peak 2 (Figure 8.13b)). This is due to the less severe condensation during peak 1. The graphs also clearly illustrate the directional dependency when considering the impact of diode distance on condensation. Top left values (blue) lay above top right values (orange) and these above bottom left values (green). This is valid for all distances up to 8.28 mm (with the exception of 7.41 mm in top right direction).

The data also indicates that up to and including the 8.28 mm distance to the diode, the heat radiation impact that the component has on the condensation is uniform. A decrease in impedance with increasing distance occurs only for distances ≥ 10.48 mm. On the basis of the created graph and with the knowledge of having definite water bridge formation for impedance values of Log(imp) ≤ 3, it is possible to identify (non-)critical regions for electrochemical migration. Based on the assumption that for ECM to occur, a closed water bridge across the 100 µm Cu-Cu gap is required (hence Log(imp) ≤ 3), "ECM-safe zones" can be calculated. These zones are valid for the specific experimental conditions. For the more moderate condensation generated on the board during peak 1, safe zones can be established for the top left and right area of the diode. These are ≤ 11.1 mm for the top left direction and ≤ 13.35 mm for the top right direction. However, for the bottom left part (green), the patterns closest to the diode already show a critical level of condensation. In the second more severe peak, a safe zone can be established only for the top left corner (Log(imp) > 3). Up to and including a distance of 8.28 mm from the diode is non-critical for ECM, as no closed water bridges form across the 100 µm electrode gap.

B. Time Domain Reflectometry to determine localized condensation

B.1 Volume and location of water droplets

The TDR measurements from the test structures with 10 µl and 30 µl water droplets are shown in Figure 8.14. The impedance is represented in relation to the position along the length of the Cu traces starting after the SMA-connectors and going until the end of the Cu traces. The impedance rising due to total reflection at the open end of the traces is not included in the graphs. The positioning of the water droplets is highlighted in blue. Highlighting in striped-red shows the high-frequency-transmission critical range of 80 Ohm and below.

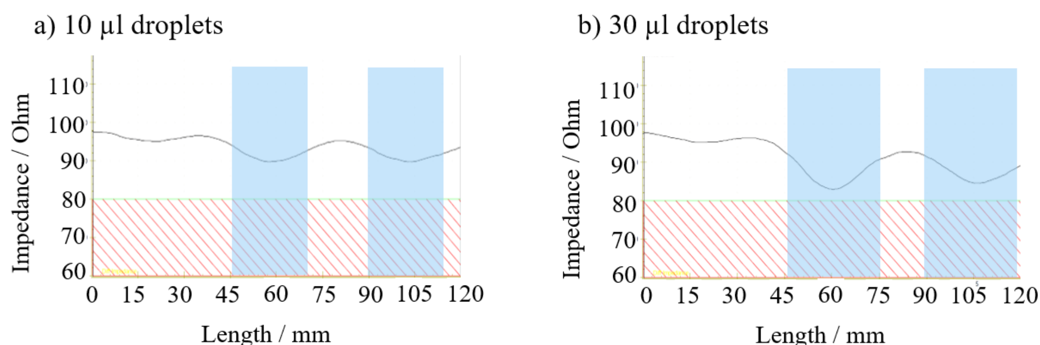

Figure 8.14: Impedance data related to length of test structure obtained from measurement with two droplets of each 10 µl water (a) and 30 µl water (b). Sections highlighted in blue describe approximate area of the droplets spreading on the test boards. Area shaded in red marks a critical impedance decrease for GHz applications.

It is clearly recognizable that both the location of the droplet along the length of the trace as well as a relative droplet volume information can be retrieved from the obtained data. The impedance for the sample with 10 µl droplets is in the range of 95-98 Ohm up to a length of 36 mm. It then decreases down to a minimum of 90 Ohm at 58 mm and rises again up to 95 Ohm at 81 mm track length. At the positioning of the second droplet, it decreases again to 90 Ohm (minimum at 100 mm). At the end of the track, it rises up to 94 Ohm. Considering a mean dry board value of 96.5 Ohm, impedance due to a 10 µl droplet drops by 7 %.

The sample with 30 µl droplets also shows an impedance between 95 Ohm and 98 Ohm up to approx. 35 mm. In the area of the first droplet, impedance decreases to 83 Ohm at 60 mm. In between the droplets, the impedance returns to 92 Ohm. The impact of the second droplet is an impedance reduction to 84 Ohm at 105 mm. Thus, the 30 µl droplets result in an impedance only 2 Ohm, respectively 4 Ohm above the transmission critical range (80 Ohm). Comparing with dry board range, impedance due to a 30 µl droplet falls by 13 %.

B.2 Localized condensation impact of flux residue

To assess the condensation-enhancing impact of the flux residue, the overall mean impedance across track length is evaluated for the bare and the contaminated structure. Impedance values are represented at distinct points over the course of the temperature profile (Figure 8.15). The mean impedance values for the clean board are shown as black square. The red circle refers to the flux-contaminated board. Minimal reached impedance values for both temperature peaks are indicated in the graph. For the contaminated board, local impedance distribution related to Cu length is given at distinct points in time (displayed in Figure 8.15a)-e)).

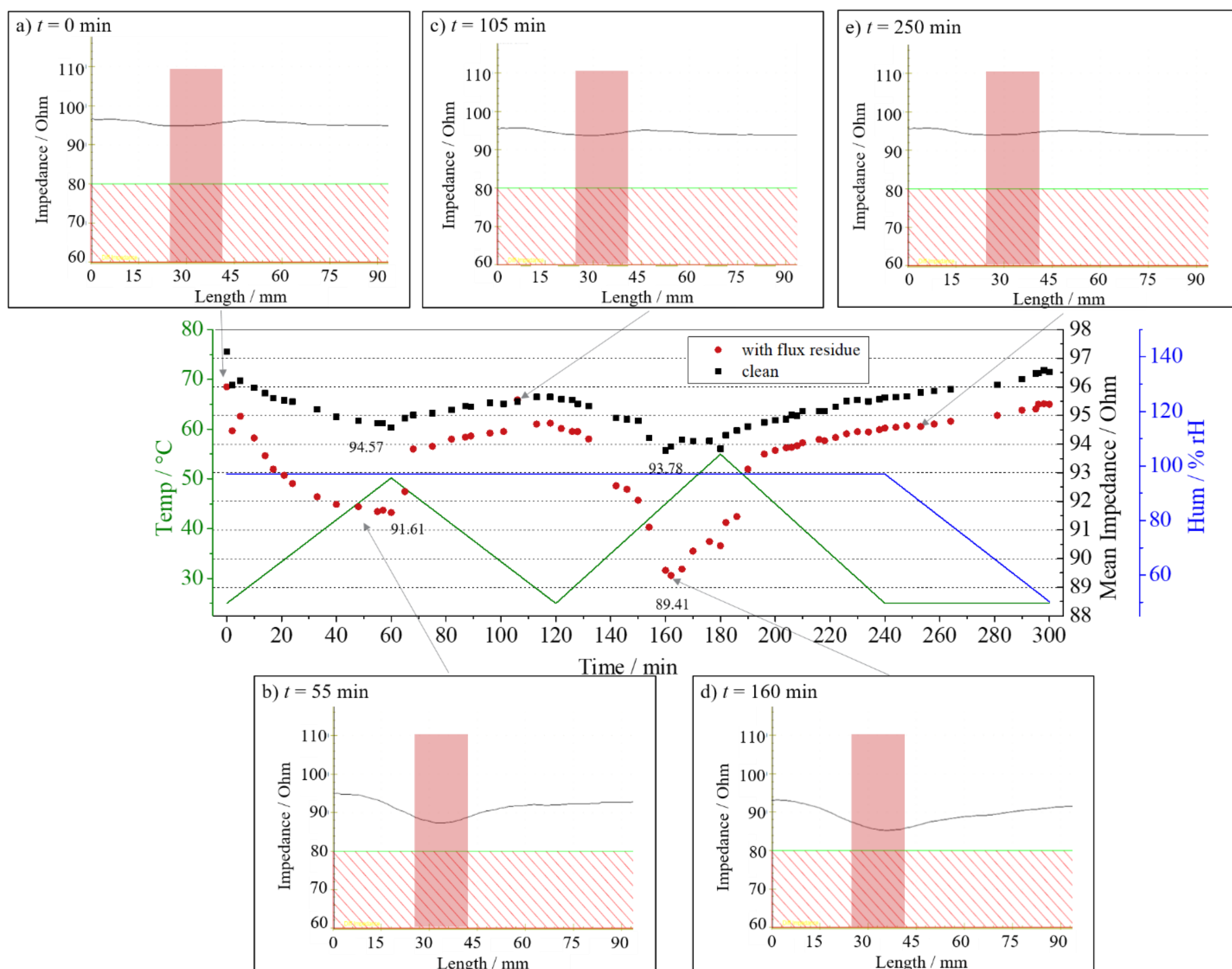

Figure 8.15: Mean Impedance for the whole length of the sample structure for both clean board and flux-contaminated board. Graphs a-d): Impedance data related to length of contaminated test structure. Highlighted red area approximates the location of flux residue.

Generally, the clean structure (black square) as well as the contaminated structure (red circle) follow the climatic profile. Impedance drops during first temperature increase due to provoked condensation and rises again once evaporation starts. The second temperature peak starting at 120 min results in another impedance

decrease for both patterns. Lower values are reached, indicating stronger condensation compared to the first peak. After temperature and humidity decrease at the end of the test, both structures increase in impedance again, reaching almost the initial values of 0 min at the beginning of the profile.

Overall, the mean impedance data shows a greater dewing for the board with flux contamination. Up to the time of strongest condensation after 60 min during the first peak, impedance of the bare board has decreased to 94.57 Ohm. The test structure with flux residue is at 91.61 Ohm at the same point in time. During evaporation, the clean structure's impedance rises in an approximately linear manner up to 95.65 Ohm at t = 120 min. Impedance for the contaminated structure increases rapidly up to 93.83 Ohm (t = 70 min). It then rises uniformly similar to the clean structure, with the exception of short-term increase to 95.54 Ohm (t = 108 min).

During the second peak, the impedance for the bare board drops to a minimum of 93.78 Ohm. At the same time, the contaminated structure drops to 89.41 Ohm. Bare board values remain in the same range until after the peak temperature is crossed and ramp down starts (t = 180 min). Values then rise linearly up to 96.52 Ohm at the end of the experiment. The impedance of the contaminated structure starts rising again already after 160 min. Starting from 200 minutes, it increases the same way as the clean structure, only remaining about 1 Ohm below until end of test.

At distinct points in time, impedance spectra across the spatial length of the Cu traces were obtained for the test structure with flux residue. The corresponding graphs are also displayed in Figure 8.15, assigned to the time of recording. For the localization of the flux residue placement, the respective area along the Cu-length is highlighted in red. The graphs overall demonstrate that TDR detects enhanced condensation at the spot of flux residue by greatest impedance decrease in this area.

The measurement obtained at the beginning of test (a) t = 0 min) shows a uniform impedance in between 95 Ohm and 97 Ohm. At a time of pronounced condensate formation (b) t = 55 min), the impedance across the whole test structure has dropped, yet the largest drop occurs in the area of the flux residue (minimum of 87 Ohm at 35 mm). After 105 min (Figure 8.15c)), the evaporation results in an impedance increase across the whole structure. Still, with values between 94 Ohm and 96 Ohm, the dry range from the beginning of the test is not fully reached. At the maximum condensation of the second temperature peak (d) t = 160 min), impedance at all positions is lowered again, while the lowest value of 85 Ohm is reached at 35 mm. In comparison with the t = 55 min data, the reduction of the impedance curve around the flux area spreads further, especially in direction of increasing length. After 250 min (Figure 8.15e)), the impedance profile related to Cu length shows values close to the initial dry state.

IV. DISCUSSION

A. Assessment of humidity impact under heating conditions using AC impedance measurements

Overall, the PCB with multiple comb structures and a heat-radiating component can be used for assessing the humidity impact at design stage of a PCBA. A layout of specific size and distinct placement of the heat-radiating component as shown in this setup can be employed to determine the extent to which the powered component can prevent critical condensation. Optimized placement of the heat-radiating component is favorable with regard to humidity robustness, which is why it is an important design aspect. Therefore, the opportunities of impedance spectroscopy to test these dependencies in a non-destructive manner for different climatic scenarios and active PCBA components is of great benefit. By means of the impedance measurement over the course of the cyclic profile, different influencing factors on the condensation process can be assessed.

The progression of condensation starts with the initial nucleation of water droplets on the substrate. This is because if water vapor is governed by a pressure greater than its saturation pressure it will transform into liquid phase to minimize its energy. The temperature of the vapor is reduced below its saturation temperature due to the contact with a cooler surface. Based on this, for the test PCB with heating provoked by the diode, the kinetics of condensation should be different depending on its closeness to the diode. However, instead of an earlier and stronger impedance drop for all structures further away from the diode, the impedance-drop to similar level shows that the first stage of condensation occurs in a similar manner for all patterns (Figure 8.8, Figure 8.9 and Figure 8.10). Initially, the impedance decreases to a stable value (approx. 1 h – 1.5 h for first temperature peak and 2.8 h – 3.2 h for second temperature peak).

This effect is supposedly due to the heat dissipation into the bulk of the PCB during the temperature cycling, which is facilitated by the aluminum plate (thermal mass causing delay in temperature change) on which the PCB is placed. Thus, the impact is equal for all comb patterns and appears to determine the early stages of the condensation process with similar impedance progression for all patterns. However, during the extended cycling test, further into the condensation, the impedances decrease depending on the distance of the structures from the diode. The lateral transmission of heat from the diode to the surrounding structures is slow compared to the vertical transmission of heat from the aluminum base plate to the PCB surface across the PCB thickness over the whole area of the board. This is an important aspect in connection with application because PCBAs in an electronic product can be attached to a heat sink as well. Under condensing conditions, it can act as thermal mass for delaying temperature changes, while the heat dissipation from a hot component occurs more slowly across the PCBA surface.

Literature also debates on early condensation effects on a surface, which are reported to be more dependent on the wetting properties of the substrate. In the case of a cooler surface exposed to high ambient humidity conditions, geometrical aspects like surface irregularities play an important role in starting initial stages of condensation [21,34]. As the condensation proceeds, the isolated droplets start to grow, meaning the mass of the condensate increases. Along with this, the enthalpy of condensation rises likewise. The latent heat of condensation needs to dissipate via the surface. If the heat cannot be released easily, the temperature of the droplet rises. This slows down further droplet growth or can even prevent it fully [21]. Impedance data progression during condensation advocates that this is a relevant phenomenon for the test case: In both temperature ramps, a difference in impedance progression related to distance to diode becomes apparent only after initial condensation has proceeded for all patterns in a similar manner (starting at 1.5 h and 3.2 h). As the condensation continues further however, the decrease in impedance and thus formation of water bridges depend on the closeness to the diode.

Based on the impedance profile during climatic cycling, the kinetics of the evaporation process can also be evaluated. . During temperature ramp down to 25 °C, all comb patterns display the drying of the surface by an impedance increase (Figure 8.8 - Figure 8.11, after 2 h and after 4 h). Upon reaching 25 °C ambient again, all patterns have reached an impedance level corresponding to their initial dry value or higher. In this range, the distance to the diode is reflected generally in patterns closest to the diode reaching highest impedance values.

In more detail, the data also suggests different rates of evaporation, depending on the distance to the diode. An initial faster evaporation of water droplets on patterns further away from the diode heating is apparent for the outermost comb patterns (A1 in Figure 8.8, G1 in Figure 8.9 and A8 in Figure 8.10, 2.2 h – 2.4 h and 4 h – 4.2 h). For these patterns, the increase in impedance happens first and with a greater slope compared to the inner patterns. The reason for this is that the vaporization presumably occurs first for droplets with larger height. The air close to the surface is thus quickly saturated with water. This needs to be balanced out first, supposedly by convection, so that the concentration gradient needed for evaporation is established once more. Only then the residual condensate, hence the smaller droplets closer to the diode can also participate in the evaporation process. Even though the initial evaporation appears prominent for a greater extent on the outermost structures, in subsequent drying, they do not reach impedance values as high as the closer patterns that are more affected by the diode heating. Also, during the drying process, it is apparent that the impedance data for all patterns show the values exceeding the initial values obtained at $t = 0$ h. This might be due to the release of the residual absorbed humidity which was initially present in the laminate, and which is baked out during the evaporation process. The porous characteristics of the FR-4 laminate make it prone to take up humidity [35,36]. The board in the test case was exposed to a relative

humidity as high as 92 %rH before and during temperature cycling; hence moisture ingress into the surface area of the laminate could occur. The knowledge that can be gained from the testing approach on the dynamics of evaporation is extremely relevant with regard to failure occurrence. The period of time for which a condensate film is present on the PCB surface greatly affects the possibilities for electrochemical reactions to take place. Accordingly, reliability of PCBA designs is significantly improved when evaporation processes are encouraged to occur fast, for example by appropriate thermal management. It is therefore important to understand the effect of heat-radiating components not only with regard to condensate formation, but also in relation to the kinetics of drying a board.

Figure 8.16 shows the humidity effect map across the PCB surface generated from the impedance data at the maximum condensation (minimum impedance) during peak 2. The color-coding shows dark blue regions for lower impedance, thus the coloring mirrors the humidity present on the surface. It shows that the heating profile around the diode is not symmetrical due to the airflow in the climatic chamber. However, the humidity effect map constructed based on the experiment can be highly beneficial for the PCBA design in order to decide on the placement of various design elements and components. In the development process and material release for automotive electronics, numerous tests are conducted without housing or with other deviations from the targeted operational environment of the device [37]. The significance for understanding testing failures at early stages is crucial for avoiding respective problems in later development stages. Conventional testing methods, especially related to humidity reliability like SIR testing often do not provide information on humidity effects on the whole PCBA surface. The generation of humidity maps for different condensation scenarios on board level can serve the establishment of “safe areas” not only around powered components that dissipate heat and have a positive impact on humidity reliability. Figure 8.16 also clearly shows the impact of diode current (0.4 A in (a) and 0.2 A in (b)) on the severity of condensation. A similar approach is conceivable for test PCBs with various assembled components that affect the surface temperature distribution. Various climatic scenarios as well as electronic operating modes could be tested in this manner and the local humidity can be mapped.

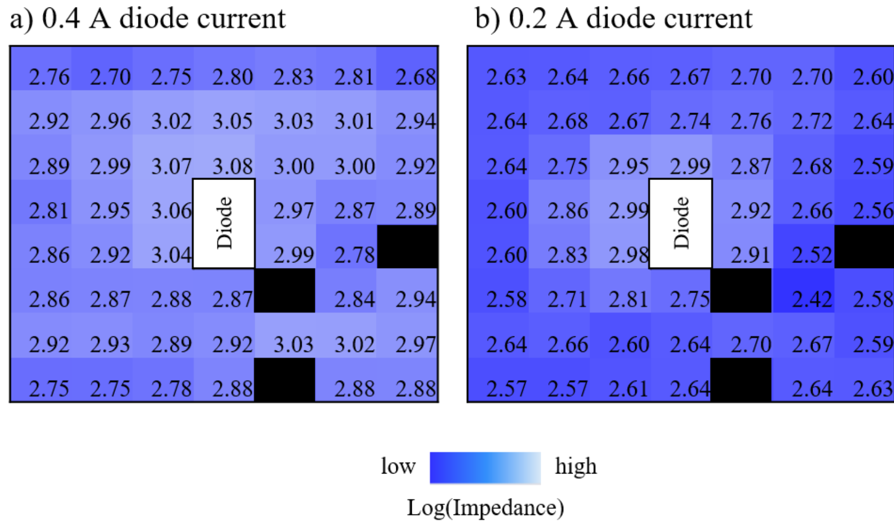

Figure 8.16: Stepless humidity impact values based on minimum impedance values reached during temperature peak 2 for a test run with 0.4 A diode current (a) and 0.2 A diode current (b). Color-coding represents level of impedance value.

B. Time Domain Reflectometry to localize condensation

Results from the TDR measurements in general show the possibility of measuring condensation for bench marking the level of condensate as a function of various parameters, which can then be used as a reference for condensation on PCBAs under various conditions. The tests conducted with 10 µl and 30 µl water droplets showed a basic possibility of assessing droplet volume in a comparative manner. As for localization, the minima of impedance along the Cu-traces was in good agreement with the actual placement of the droplets.

A similar observation was made for the comparative test of bare board and flux contaminated board in a cyclic condensation scenario. Data of the mean overall impedance was clearly able to distinguish a mean moderate condensation on the clean board and the more severe condensation established by introducing contamination. It was shown that in principle, just like with the AC impedance technique, the pulsed method is able to sense adsorbing and desorbing humidity as well. In case of the test samples, the condensation and evaporation processes via TDR could even be detected with transmission lines covered by a solder mask layer. In addition, the localization function of the technique could be employed to confirm strongest water adsorption at the area of flux contamination. The local resolution of TDR measurements depends greatly on the material transitions with different dielectric properties. In the present case, the solder mask covering of the traces is detrimental for measurement quality, even though it represents a real-life condition.

C. General assessment of humidity detection

Overall, the results show the possibility of gaining detailed information of humidity effects on a PCB with relation to PCB design characteristics. The establishment of a cause-effect relationship of influencing parameters like surface temperature or contaminants on water film formation is advantageous both in early development stages for products and processes as well trouble shooting for existing products. The option to test humidity interaction non-destructively is additionally helpful, because the repeated testing with slight variations of climatic conditions or other impact factors is possible.

The use of AC impedance as detection method to evaluate different condensation levels with distance-relation to a heating component was found to be useful. Even though the experimental conditions underlay the non-uniformity of heat distribution, the general feasibility of the approach allows non-destructive testing for a number of variants, e.g. component heat outputs with regard to severity of water film buildup. The related humidity effects can be studied and related to the risk of corrosion failure. This approach is especially valuable in early design stages of product development, as a timely recognition of critical designs can be achieved. The placement of active components that are favorable in avoiding severe condensate formation can be adapted for example close to narrow-pitch PCB patterns or similar designs that are prone for humidity-induced failure. TDR measurements could provide information on the localized condensation formation and volume effect.

V. CONCLUSION

1. AC impedance measurement of a matrix circuitry of comb patterns in local vicinity of a heat-radiating diode on a PCB surface can be used to evaluate a condensation risk at early design stages of PCB development. It was shown that impedance values of condensate sensing patterns can be divided in ranges, indicating a dry surface, intermediate condensate formation and ECM-critical water bridging to assess migration risks.

2. In case of a distinct heat distribution on a PCB surface because of a powered component, the test setup demonstrated the possibility of calculating ECM-safe distances. For the event of inhomogeneous heat distribution and for the test conditions given in this study, a 0.4 A powered SMT diode prevents critical water bridging of 100 µm gaps of up to 13.35 mm, depending on direction.

3. TDR was used as a non-destructive method to determine local condensation on solder mask-covered Cu-traces. Using this method not only enabled a local identification of droplets but it could also be used to obtain a proportional determination of droplet volumes.

4. The presented test methods and setups can serve the purpose of evaluating various active and passive PCBAs and material related reliability in relation to humidity interaction. Results could be used in the early stage development, for example in layout guidelines of a board, to significantly improve thermal management or in qualification processes of new materials like solder pastes.

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9. ON THE FEASIBILITY OF ELECTROCHEMICAL IMPEDANCE SPECTROSCOPY TO ASSESS CLIMATIC RELIABILITY OF PRINTED CIRCUIT BOARD ASSEMBLIES

Simone Lauser, Theresia M. M. Richter, Vadimas Verdingovas, Rajan Ambat

Abstract – This paper focuses on the feasibility of Electrochemical Impedance Spectroscopy (EIS) to assess the humidity robustness of Printed Circuit Board Assemblies (PCBAs). The method is analyzed based on the data from different experimental conditions. The general feasibility of detecting the formation of a water layer on a PCB surface by tracing changes in resistive and capacitive parameters of the system is described. In contrast with conventional DC testing methods like Surface Insulation Resistance (SIR), it is demonstrated how EIS can be used to evaluate the criticality for Electrochemical Migration (ECM) without actually producing electrochemical migration failure. Within this scope, the presented work contributes to the investigation of EIS as a standardized method for evaluating climatic reliability of electronics, overcoming drawbacks of conventional DC SIR measurements.

Keywords – Electrochemical Impedance Spectroscopy; water film formation; electronic reliability; humidity, electrochemical migration, Surface Insulation Resistance

I. INTRODUCTION

Reliability of electronics under harsh exposure conditions is of considerable importance. Continuous miniaturization, higher packaging densities and multi-material use for Printed Circuit Board Assemblies (PCBAs) has significantly increased the humidity related issues on electronics. External climate related reliability issues are especially prominent in the automotive electronics field due to exposure to extreme conditions connected to the use [1]. Among the humidity caused failure modes, one of the biggest concerns is the phenomenon of electrochemical migration (ECM). It is a humidity related failure mode, meaning the prerequisite for an occurrence is the presence of a humidity film on the PCB [2,3]. Conducting tracks, component pins or other structures on the PCB can serve as anode and cathode, once a DC potential is applied to them. With a water bridge in between them, the metal ions (e.g. Sn, Cu or others) dissolve from the positively biased electrode and are transported to the cathode due to the electric filed. At the cathode, the metal ions are reduced. Due to the field-assisted deposition process, they deposit in the form a dendrite growing from cathode to anode. Given enough time, the dendrite can bridge the gap between the electrodes establishing an electrical connection [4]. This in turn can result in the malfunction of the electronic assembly, including flying sparks on the PCBA if burning of the dendrite occurs. Many metallic materials on the PCBA are susceptible to ECM.

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Among them are silver, tin, copper, nickel, or gold, which are either part of the solder material or exist on the PCBA as surface finish or conductive tracks. Further, the effect of humidity and ECM probability is accelerated if contamination like flux residues from the manufacturing process are present on the PCBA surface [2,5–8].

Since the prerequisite for humidity related failures on a PCBA including ECM is the formation of the water film to a substantial thickness, it is important to understand the gradual buildup of the water film under specific conditions. This information could then be related to ECM-criticality. Unlike in other conventional corrosion issues, electrochemical cell formation on the PCBA surface is electrolytic in nature, as the applied potential bias between points results in cell formation under water film conditions. The water film acts as an electrical conducting layer over the PCBA, and the current leaking through the water film (generated by the electrochemical process) causes functionality issues, and can eventually lead to ECM. In this context, the thickness of the water film is a crucial impact factor. The electrical capacity of the water film as it grows is what determines the kinetics of electrochemical reactions and the transition to failure.

Evaluating the climatic robustness of the various components and design elements in connection with PCBs or the device as a whole is an important part of electronics device development, particularly in automotive industry. Materials and designs as well as manufacturing processes need to be qualified for their effects related to exposure to various climatic scenarios. The conventional method to approach corrosion failure modes in automotive electronics development is the Surface Insulation Resistance (SIR) test. It is a DC based approach, meaning potentials ranging from 5 V up to 1250 V are applied to test patterns under different climatic conditions [9,10]. The high voltages provoke dendrite formation in distinct humidity environments. This failure mode is identified by a decrease in resistance between the oppositely biased design elements. Different industry standards define threshold values, such as SIR > 10^8 Ohm as pass criteria for PCBAs under test [11]. A major drawback of this method is not only the fact that it is destructive to the sample and thereby prevents the repeated use of a specific design for different climatic scenarios. The DC potential also leads to polarization of the electrodes and consequently impedes the detection of gradual water layer buildup by distinguishing different conduction mechanisms [12]. To overcome these issues, AC based approaches such as Electrochemical Impedance Spectroscopy (EIS) can be employed. The method relies on the application of a small alternating voltage signal, which does not impose significant overpotential to the sample. The response is a frequency-dependent impedance, delivering information on the resistive and capacitive properties of a system under test, and specifically for this case the detailed electrical property of the water film [13–15].

In relation to humidity effects on electronics, the use of EIS has been reported for elucidating various effects especially in connection with flux residues. Flux residues are known to enhance corrosion criticality due to their hygroscopic character and the increased conductivity they provide in a water film. By means of EIS, their corrosion potential can be assessed, for example in connection with copper layers in different condensation scenarios [16,17]. Comparing with the standard SIR technique, EIS has been shown to provide information on the characteristics of the electrolyte that provides the pathway for ECM as well as on the buildup of the electrolyte film itself [18,19]. However, none of these works looked at EIS comprehensively as a method for testing humidity effects on electronics in comparison with the presently used DC technique. Likewise, no demonstration on how the results from EIS can be interpreted to provide detailed information on the water film buildup and transition to a critical point that can lead to ECM has been made. An extensive consideration of advantages and disadvantages of using EIS instead of DC methods is required for determining the feasibility of the method. To achieve this, the predictability of possible DC failure of design using EIS without subjecting to the destructive DC testing needs to be outlined.

This paper reviews EIS as a feasible method for understanding the water film buildup on electronics such as PCBAs. In relation to the water film effects on reliability, the EIS method is contrasted with the presently used DC methods for climatic reliability testing. The work presented in this paper is a combination of results from the research activities carried out by the authors together with the review of results from the authors' previous publications and related literature, with the idea of providing a comprehensive analysis of the feasibility of the method. In order to provide comprehensive analysis, the paper is segmented in three sections as follows: (i) Part 1 summarizes the information on the role of gradual thin water film formation on a PCBA surface and its influence on the corrosion reliability. Influencing factors related to the water film buildup are summarized, and the process of water bridge formation, leading to a continuous water film connecting contacts on a PCB surface is described. A general application of EIS to detect the condensation is compared with the conventional DC testing approach, (ii) Part 2 provides complementary investigations carried out to further correlate the possibility of using EIS for assessing the DC-provoked ECM failure. Different PCB test geometries with regard to layout are used in the described experiments and results. Test PCB geometries with polymer and ceramic substrates are described in order to show the adequacy of EIS measurements for general PCB assembly and for interconnect PCB types with different design elements. By directly contrasting it with the DC method, this part of the paper is to show how EIS can be used to predict critical states for dendrite growth under DC conditions. This is an important step towards bridging the gap of using EIS as a method for humidity robustness testing. (iii) Part 3 of this paper describes a case study of EIS use for the next level of testing, which is the usage of assembled boards with soldered

components. In a cyclic temperature test based on an international standard, EIS and DC approaches are contrasted. This comparison shows how the EIS method can deliver additional information in conventional tests using PCBs with assembled components.

II. PART 1: GENERAL INFORMATION ON THE FEASIBILITY OF EIS AS A TEST METHOD FOR HUMIDITY ISSUES IN ELECTRONICS

In the context of the reliability of electronics, humidity-based failures are a regular problem. The main component of most automotive electronics, the PCBA, faces numerous different climatic environments during its lifetime. Many of them can lead to condensate formation on the surface. The occurrence of thin water layers can trigger various corrosive processes, a prominent one is ECM [20]. As it only requires a thin condensate film, it differs from conventional corrosion issues such as corrosion in sea water or in soils [21]. For this reason, in the PCBA context, a detection possibility of condensate formation as prerequisite for failures is preferable. In particular, the understanding of transition points in buildup of a connected water bridge between electrodes as a requirement for ECM needs to be considered a crucial factor for evaluation (see Figure 9.1) [22].

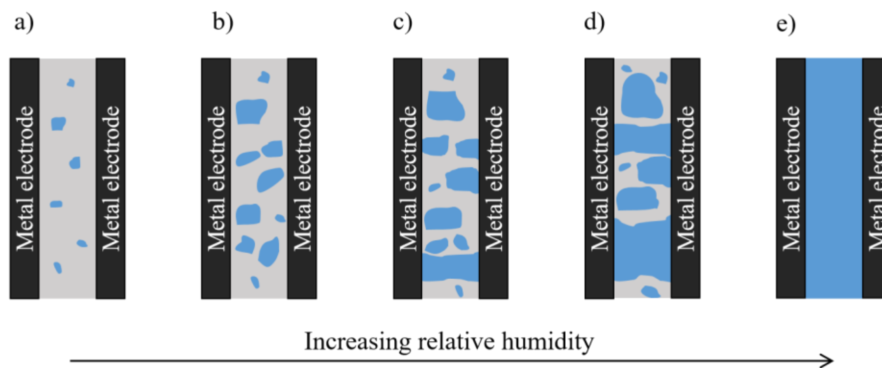


Figure 9.1: Schematic representation of condensation and water bridge formation between two metal contacts on a substrate surface [22].

Once it has built up, the characteristics of the water film strongly influence the corrosive processes. Among the important parameters are the conductivity of the film as well as its established thickness. The thickness and uniformity of the electrolyte layer also play a key role when evaluating the ECM risk. A pronounced bridging of a metal gap by the water film allows the dendrite growth from anode to cathode.

To determine humidity assisted water film formation and progressive evolution of failures, different approaches can be followed. These range from the development of micro-sensors for dewing events based on silicon integrated capacitors to indium nitride devices that detect condensation by water droplet formation in the transistor gate region and consequent current changes [23,24]. Also sensory concepts

premised on Surface Plasmon Resonance and hence a change in refractive index of a medium during condensate formation are widely used [25]. Additionally, measurements of surface temperature to detect reduction below the dew point or in-situ imaging of the surface are possible alternatives. However, a relation of the water film formation with the corrosive failure that it enables is not feasible with these approaches.

Testing climatic reliability in development phases in the automotive context is supposed to cover all humidity interactions that a PCBA-setup can face in the field. Many verifications involve accelerated tests that go beyond actual field load, like the K15a dewing test [10]. Regular testing that is performed in various stages of the development process is the SIR test. The approach is defined, among others, in the IPC-9202 standard [26]. In order to represent actual products, design for SIR testing involves various test board layouts. These range from standard copper comb patterns on PCB-laminate towards more extensive assemblies with soldered components [10,27–29]. Based on a drop in surface insulation resistance below a defined threshold, the occurrence of a corrosive process, like a dendrite short, is evaluated. The SIR test comes with the advantage of a comparatively simple measurement technique and the possibility to apply the test easily to a variation of sample patterns, evaluating board cleanliness, durability of coatings, and solder joint reliability. However, as mentioned in numerous of SIR literature studies, the method also has its drawbacks. A major disadvantage is the fact that the SIR test is destructive to the specimen due to the applied DC voltages. Samples cannot be re-used after testing and thus for every climatic scenario to be tested, a new sample buildup is required, pushing the cost for investigations. In addition, the SIR test is susceptible to detection of pseudo-failures. As the failure criterion is simply a reduction in surface resistance, test failures occur for example due to dirt such as fibers that short-circuit test patterns [28]. Therefore, careful examination of the failed samples after testing is necessary in order to ensure the presence of dendrite failures. However, the occurrence of the ECM failure can also be intermittent during testing, meaning a dendrite under a transient water film can burn away after the evaporation and no trace of the failure is left on the board for analysis. This hampers the allocation of a cause-effect relationship for corrosion failures. A particular handicap of the SIR test is also the fact that the application of the DC voltage leads to polarization of the electrodes and thus impedes gradual detection of water film buildup. Thus, the technique cannot deliver the information on the particular conditions that lead to the failure [19]. Similar methods to assess ECM like the water drop (WD) test, the temperature humidity bias (THB) test or the thin electrolyte layer (TEL) test are based on the same principles and therefore not capable in displaying the stages in condensate formation that lead to ECM [30].

An alternative approach is the use of AC-based methods, such as Electrochemical Impedance Spectroscopy (EIS) [31]. EIS is a measurement method that relies on the application of a small alternating voltage signal (mV-range) to the specimen. A broad band of frequencies can be used to assess different resistive and

capacitive properties of a system. The response of the system to the alternating excitation is a function of the complex impedance of the system. The resistive part is dependent on the area of the electrodes, their distance and the specific resistance of the medium between the electrodes. The capacitive reactance depends on the regarded frequency and the permittivity of the system. Specific resistance and permittivity change with ongoing condensation. This enables monitoring of gradual water film buildup, for example on a test PCBA surface. In interpretation of EIS data, it is possible to consider a specimen in its surrounding as an electrical equivalent circuit with different resistive, capacitive or inductive elements. Effects like the double layer formation at an electrode-electrolyte interface can be represented by a capacitor. The charge transfer resistance at the interface or the impedance of an electrolyte itself can be understood as resistors. The constant phase element (CPE) represents an imperfect capacitor, with partially resistive properties [32–34]. The observation of changes in equivalent circuit parameters allows tracing of the condensation process up to water bridge formation between PCBA design elements. The Bode plot, showing system impedance |Z| and phase shift over the measured frequency range, is often used for representation of data. Another alternative is the Nyquist Plot, giving real Part *Re* and Imaginary Part *Im* for all measured frequencies [15].

In Figure 9.2, the water film formation between two electrical contacts on an FR-4 laminate is schematically represented with electrical equivalent circuits and Bode plots for each stage. In dry stage (Figure 9.2a)), the system can be represented as parallel circuit of a capacitor and a resistor, governed by the FR-4 laminate ($C_{FR\text{-}4}$ and $R_{FR\text{-}4}$). The strong capacitive behavior of this state is mirrored by the −90° angle going into high frequency domain. The impedance |Z| is prominent for low frequencies, it decreases with increasing frequency. Once condensate has built up on the surface (Figure 9.2b)), this uneven distribution of water can be represented in the equivalent circuit by additional elements. The water layer affects the laminate capacitance ($C_{FR\text{-}4+WL}$) and the resistance is only governed by the water properties (R_{WL}). The CPE Q_{DL} represents the double layer that has built up at the electrode-electrolyte interface. Also, the R_{CT} charge transfer resistance needs to be considered at this point. As the condensate itself is non-homogeneous and barely touching at some spots, a solution resistance R_S as well as CPE Q_S can be integrated into the equivalent circuit to display the issue of transferring charge from one water island patch to the other. In the Bode Plot, this stage is mirrored in impedance by generally lower values across the whole frequency spectrum. In the intermediate and higher frequency domain, the phase shift is moving towards less negative values, and therefore also represents the deviation from purely capacitive behavior, as the system shifts into resistive character due to the water adsorption. Once a complete uniform water film of pronounced thickness bridges the gap between the metal contacts, the solution resistance and CPE of the solution can be eliminated (Figure 9.2c)). The system now has a largely resistive character, determined by the kinetics of diffusion of species through the water film and charge transfer in transition from ionic to electronic

conduction at the electrodes. In the Bode Plot, this is displayed by a considerable impedance drop and phase shifts in the 0° range in the intermediate frequency domain. Correspondingly, a number of EIS parameters can be used for an extensive evaluation on how pronounced the water film buildup between to metal contacts on a PCBA surface has occurred. When performing EIS measurements, depending on need of holistic investigation, the equivalent circuits can become increasingly complex to understand processes in detail. However, they can be simplified to focus on trends, for example to show fundamental changes in resistive or capacitive properties in a changing system.

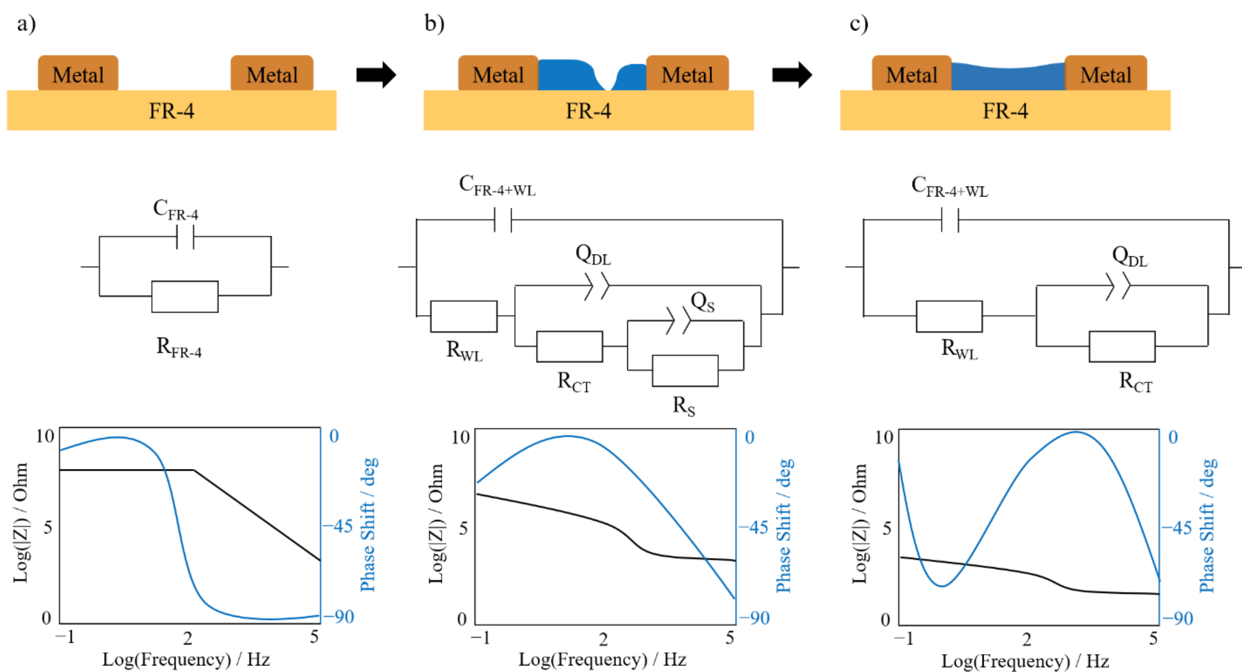


Figure 9.2: Graphical representation of water film buildup between metal contacts on a FR-4 surface with appropriate electrical equivalent circuits and schematic Bode Plots.

The mentioned technical possibilities of impedance spectroscopy have come to use in various humidity related corrosion problems. Other than the mentioned assessment of flux residue corrosiveness, dew point corrosion can be studied as well. Likewise, the establishment of a film with "bulk water behavior", providing a continuous pathway for ECM is also describable by low impedance values (single-digit-kOhm region) and high phase angles (close to 0°) [16,35–37]. The characterization of conduction mechanisms in electrolyte layers comprised of a thin water film with flux residues can be measured and evaluated by EIS. By means of model generation and electrical equivalent circuit fitting based on measurement data, it is possible to distinguish between the sole resistance of the water layer between two electrodes and the electrochemical processes occurring that the electrode-electrolyte interface [19].

Accordingly, in comparison with the conventional DC measurement, EIS delivers more comprehensive information on the system under investigation. It is a high precision technique and very sensitive towards humidity changes involving changes in dielectric properties of a specimen [32]. However, the approach is not used widely as an evaluation method for PCBA climatic reliability. Still, there is wide spread interest to use EIS in the industry as a supplement or substitute for the DC measurement. However, the fact that there is no clear allocation of EIS parameters to assess ECM-criticality in the case of DC application poses a problem for the implementation. In order to evaluate the EIS method as alternative for the conventional DC testing, it needs to be contrasted more in detail with the SIR measurement. Some studies have already demonstrated the need for this comparative assessment, along with the benefits that come with it. It has been found that the effect of the ion depletion at the electrodes due to the strong DC signal can be circumvented by using AC potentials instead. In addition, it was demonstrated that it is possible to correlate impedance and phase shift values with leakage current development hinting to ECM. This is shown in Figure 9.3 for a condensation experiment on boards contaminated with glutaric acid. Criticality displayed in increased leak currents are also reflected in the EIS by reduced |Z| and phase shift towards 0 angle [19,35,38].

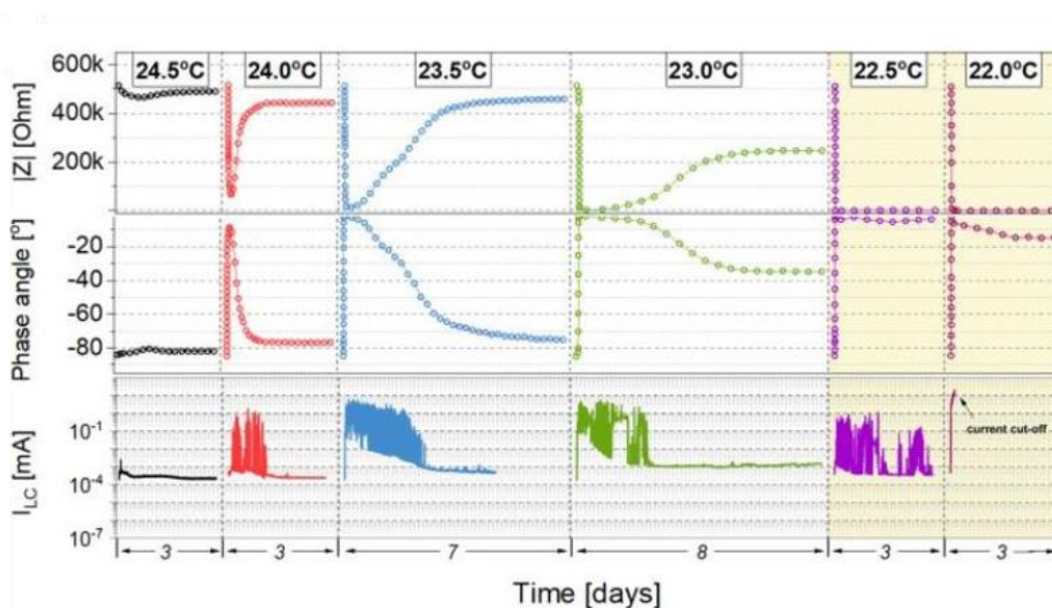


Figure 9.3: Impedance, phase angle and leakage current data for an active condensation experiment at a 25 °C/80 %rH ambient on SIR patterns contaminated with glutaric acid [35].

III. PART 2: COMPLEMENTARY WORK FOR A COMPREHENSIVE UNDERTANDING OF THE TECHNICAL OPPORTUNITIES OF EIS MEASUREMENTS IN REALTION TO CONVENTIONAL DC TESTING

In this part, the EIS technique is compared to the conventional DC measurement in determining the water film buildup, leak current, and finally ECM failure on the basis of various experiments. Results presented are a combination of a summary of authors' published work in this area together with some additional experimental results to prove the feasibility. As conventional climatic testing in material release processes for PCBAs are based on application of a DC potential, it is the goal to compare EIS as an alternative method for this application in experiments. In the results presented below, by alternating EIS and DC measurements on the same pattern, the required water amount that is needed to establish dendrite formation is detected by EIS. The underlying idea is that EIS mirrors the humidity status on a PCB surface at all times, which can then be used to predict a critical condition for ECM if DC bias exist on the PCBA surface. In order to achieve a precise allocation of EIS threshold values that indicate an ECM risk, a number of studies on test patterns with different geometries and materials has been conducted.

Testing of the described work has been performed as intermittent mode of EIS and DC on the same sample, as schematically shown in Figure 9.4. This approach allows precise correlation of information from both measurements. Climatic testing was carried out using a cycling temperature profile to provoke condensation on the sample surface. In other mentioned work, condensation was achieved by fixing the samples to a Peltier cooling stage and actively cool them below dew point. By alternating the EIS technique with DC steps, in which a fixed potential is applied to the test specimen, it can be verified whether the water film is already pronounced enough to enable ECM. These sequences are employed until dendrite shorting of the electrodes occurs in a DC step, indicated by a strong rise in Leakage Current level above 1 x 10^{-2} mA. Allocation of EIS parameters from the previous step enables determination of threshold values that indicate the ECM-critical water layer thickness and bridging characteristics.

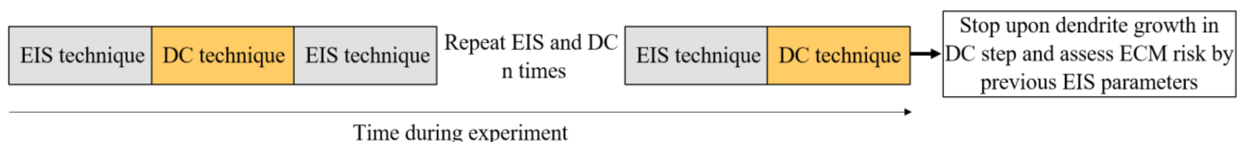


Figure 9.4: Schematic representation of intermittent EIS and DC testing to assess the water film status that is needed for dendrite growth upon DC application.

Experiments using laminate

In previous work, condensation testing was performed on standard SIR-comb pattern layouts. Copper patterns with different gap sizes (100 µm, 200 µm and 300 µm) on FR-4 laminate, in one variant also with solder mask in between the gaps, were used to assess an ECM-critical water film non-destructively by EIS (Table 9-1).

Table 9-1: Sample pattern variations used for EIS with intermittent DC testing to assess ECM failure.

Type	Sample Description
A	200 µm Cu-Cu distance, FR-4
B	200 µm Cu-Cu distance, solder mask
C	100 µm Cu-Cu distance, FR-4
D	300 µm Cu-Cu distance, FR-4

For this approach, active cooling of the samples below dew point in order to establish different levels of water film was performed. Cooling profile time was varied for some of the tests in order to verify DC and EIS correlation for different climatic scenarios. During condensation and ECM, changes in the EIS-signal were evaluate to define threshold values that indicated the possibility for dendrite-shorting upon DC application. The analysis demonstrated that a significant change in EIS was prominent before dendrites occurred under DC. The sequential condensation and water film buildup on the substrate in between the comb patterns was mirrored in resistive and capacitive changes across the complete tested frequency.

The DC leakage current behavior could be classified according to three regimes: (i) “dry” region (leakage current $< 1 \times 10^{-4}$ mA), (ii) “condensation” region (leakage current $\geq 1 \times 10^{-4}$ mA and $< 1 \times 10^{-2}$ mA, mirroring water droplet accumulation between the electrodes) and (iii) “dendrites” region (leakage current $\geq 1 \times 10^{-2}$ mA, indicating dendrite shorting of electrodes). To allocate with the EIS measurements, these domains were related to distinct EIS impedance values. A compilation of these results is shown in Figure 9.5 for four different types of samples (A-D). With regard to ECM-criticality, it was shown that a water film pronounced enough to enable dendrite growth (“dendrites”) could be described by a 68 kHz EIS-impedance of $\leqq 2 \times 10^4$ Ohm. This value was valid for all tested patterns, independent of the tested Cu-Cu distance and climatic scenario that lead to condensation.

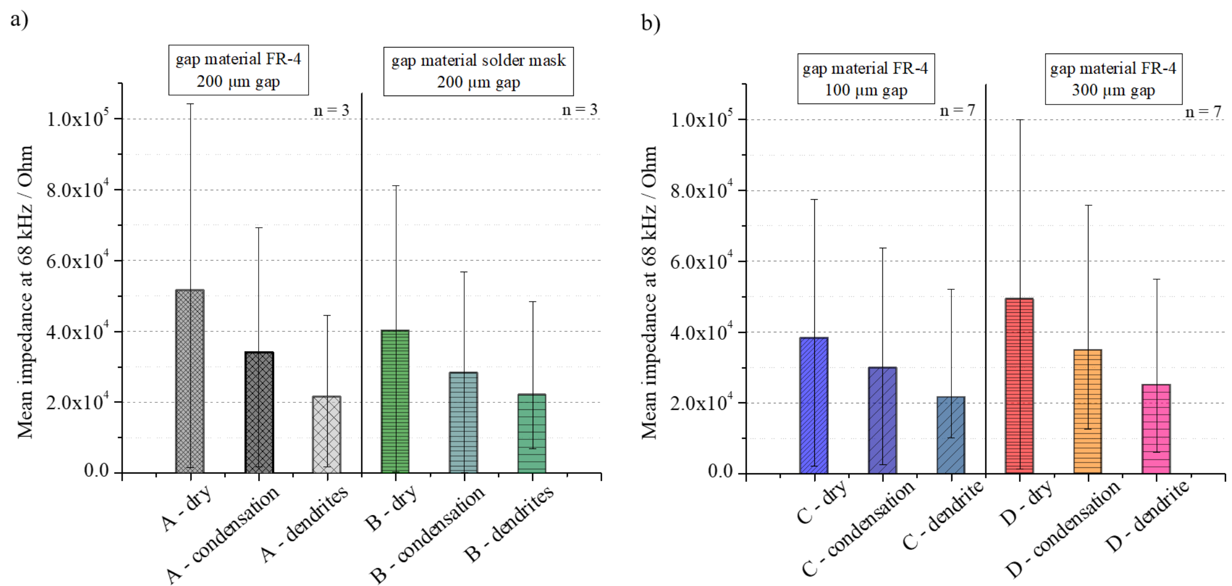


Figure 9.5: Mean impedance values for intermittent EIS and DC condensation testing for different samples types (A-D), related to “dry”, “condensation” and “dendrites” leakage current regimes.

For a closer understanding of the water layer detection capability of the EIS approach, further tests have been conducted using single geometry design on a FR-4 laminate surface. Figure 9.6a) shows the test pattern used for this purpose, which consists of two opposing T-shaped Sn-structures serving as electrodes. Sn-trace width was 200 µm, with the two T-shapes facing parallel for 600 µm with a gap size of 125 µm. Substrate material for the test structure was FR-4 laminate with 1.6 mm thickness. In order to obtain dew formation on the sample surface, a climatic profile (Figure 9.6b)) was imposed on the patterns in a temperature and humidity chamber. (SH-242, ESPEC Corp., Japan). Humidity was ramped up to 95 % rH, while temperature was kept at 25 °C. Temperature was then ramped up to 40 °C over the course of 30 minutes. Ramp down time was also 30 minutes. The second temperature peak of 60 °C was controlled over the course of 60 minutes ramp up and ramp down time. Condensation on the samples was provoked by the strong temperature increase of the ambient and the fact that the sample lagged in temperature adjustment. The effect of a cooler surface compared to ambient climate was enhanced by mounting the sample on an aluminum heat sink.

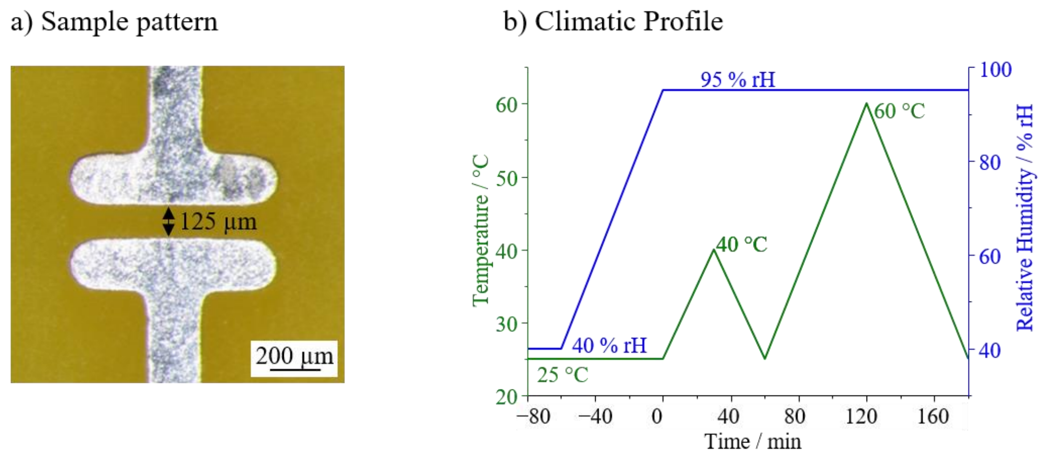
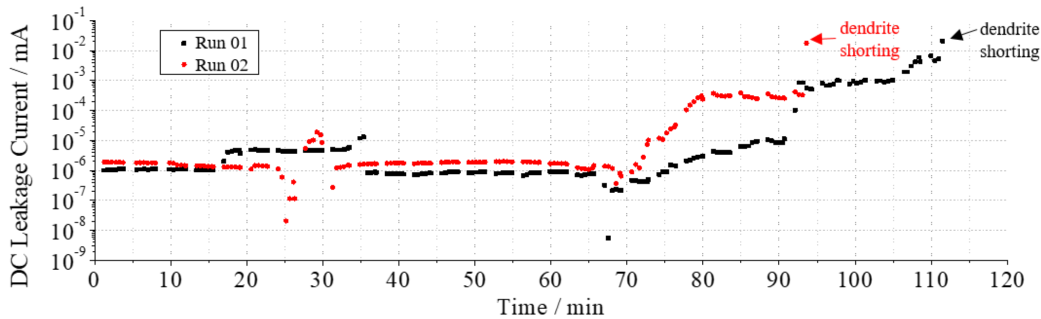
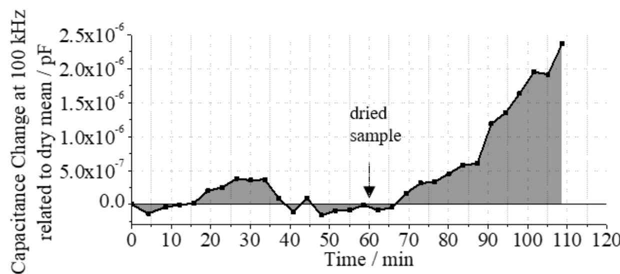


Figure 9.6: a) Test Pattern with two opposing T-shaped Sn structures of 125 µm gap used for alternating EIS and DC measurements. b) Climatic profile that the test patterns were subjected to in order to provoke repeated condensation and evaportion on the surface.

During climatic cycling, a measurement sequence of alternating EIS and DC measurements was performed (starting at $t = 0$ min in Figure 9.6b)). A 12 s EIS-sequence was comprised of four scans from 10 kHz to 100 kHz with an AC amplitude of 10 mV. It was followed by a 30 s WAIT-sequence, where no signal was applied to the pattern. Following DC was performed at 10 V application for 180 s. After another 30 s WAIT period, EIS was started again. By alternating the measurement modes, it was possible to assess the water bridge buildup causing changes to the EIS signal. The each following use of the DC was to test whether the buildup was yet pronounced enough to form dendrites across the gap. The experiment was repeated twice with each new specimen. EIS-data was analyzed by means of considering the system as an RC-parallel circuit. The capacitance change at 100 kHz related to the dry mean value of four EIS-scans prior to starting the climatic profile was evaluated. Figure 9.7 shows the results of both runs from the intermittent DC and EIS testing, whereas a) shows the DC current for both runs, and b) and c) each the capacitance changes for run 01 and run 02, referred to as *Cp*. By means of signal progression, the humidity status of the surface can be retraced.





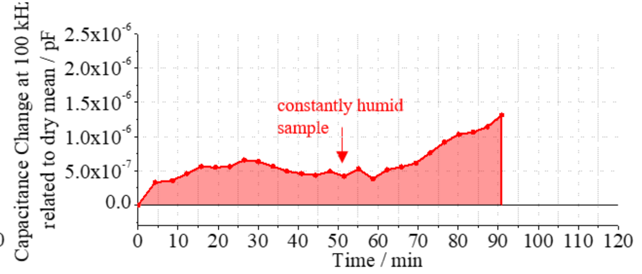


Figure 9.7: a) DC Leakage Current progression during climatic cycling up to dendrite shorting for Run 01 (black) and Run 02 (red). The capacitance change related to the dry mean value is depicted in b) for Run 01 and in c) for Run 02.

Both DC and EIS data show changes in characteristics with change in the climatic profile (Figure 9.6b)). Leakage Currents increase about one order of magnitude, from 10^{-6} mA to 10^{-5} mA during the time of the first peak ($t \approx 30$ min). The increased value range is temporally extended for Run 01 (black), compared to Run 02 (red). After 40 minutes, both curves have returned back to their initial value range. After approx. 70 minutes, the impact of the second temperature ramp up is visible. Current in Run 01 increases in two steps: up to a level of 1 x 10^{-5} mA from 70 – 90 minutes. It then jumps two orders of magnitude and holds this range, before another moderate increase starting after 92 minutes is followed by dendrite shorting at 112 minutes. Current in Run 02 rises first from 70 – 80 minutes, and then remains at a stable range of 3 x 10^{-4} mA for twelve minutes, while dendrite shorting occurs after 92 minutes.

The data of parallel capacitance *Cp* change at 100 kHz for both runs is clearly distinguishable. In Run 01 (Figure 9.7b)), *Cp* reaches a dry state with very low values when the temperature has ramped down from the first peak. Between 45 minutes and 65 minutes, the value is below the baseline, indicating a dried sample. After approximately 65 minutes, the capacitance rises up to a value of 2.23 x 10^{-6} pF, before dendrite shorting occurs in the following DC step. *Cp* in Run 02 (Figure 9.7c)) does not return to the dry baseline anymore after first temperature peak. It remains at a level of at least 4 x 10^{-7} pF (60 minutes) and continues to slowly increase up to DC dendrites after 92 minutes.

Correspondingly, the EIS-signal indicates that some amount of humidity is present on the sample during the whole course of the experiment. This is however is not distinguishable from the DC experiment.

Experiments using ceramic substrate

An additional study was conducted on comb pattern on LTCC (a Glass-Al_2O_3-Ceramic) surface to study the impact of surface on the condensation process and the detectability of EIS. AgNiPdAu was used as metallization. The track width was 200 µm and the gap size was 300 µm (Figure 9.8a)). In order to assess EIS feasibility to evaluate humidity level changes, the samples were brought into high humidity ambient. They were exposed to a maximum of 97 %rH, and a temperature ramp to provoke surface adsorption of water by a temperature difference between ambient and LTCC surface (Figure 9.8b)).

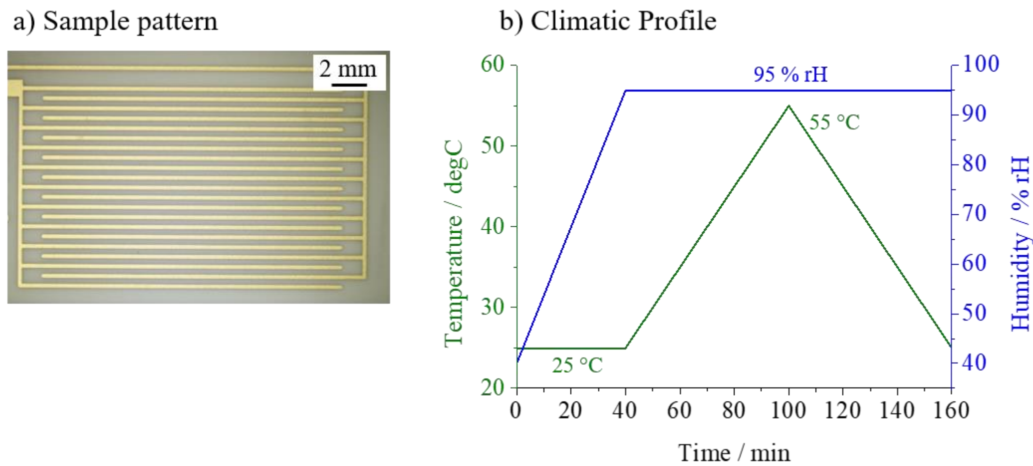


Figure 9.8: a) Photograph of interdigital comb pattern on LTCC surface, b) Climatic Profile used for EIS-and DC-evaluation of LTCC substrate.

Three experiment runs of EIS with intermittent DC testing were performed during the progression of the climatic profile with each new samples. An EIS-sequence was conducted as four scans between 10 kHz and 100 kHz frequency. The duration of a sequence was approx. 12 seconds. DC was performed for 3 minutes at a potential of 10 V. Between cycling the methods, WAIT periods of 30 s were established.

Over the course of the temperature cycling, the DC Leakage Current was evaluated. EIS-data was analyzed by means of the capacitance change at 100 kHz, related to the dry mean value of four EIS-scans prior to starting the climatic profile, similar to the approach described on the previous section on FR-4 laminate (Figure 9.9). The leakage current remains stable in the 1.5×10^{-6} mA region for all runs until $t = 350$ minutes. Afterwards, a 30 minute prolonged increase by two orders of magnitude is detected (maximum of 2.7×10^{-4} mA in run 3). In the same manner, the currents decrease again and stabilize in the initial 1.5×10^{-6} mA range. The Capacitance deviates from its 0-baseline in the same region during the

climatic profile. A stable increase for all runs occurs up to approx. $0.5 \cdot 10^{-6}$ µF. Currents as well as capacitances return to their initial value at the end of test. Subsequent optical inspection confirmed that no dendrite growth occurred during testing.

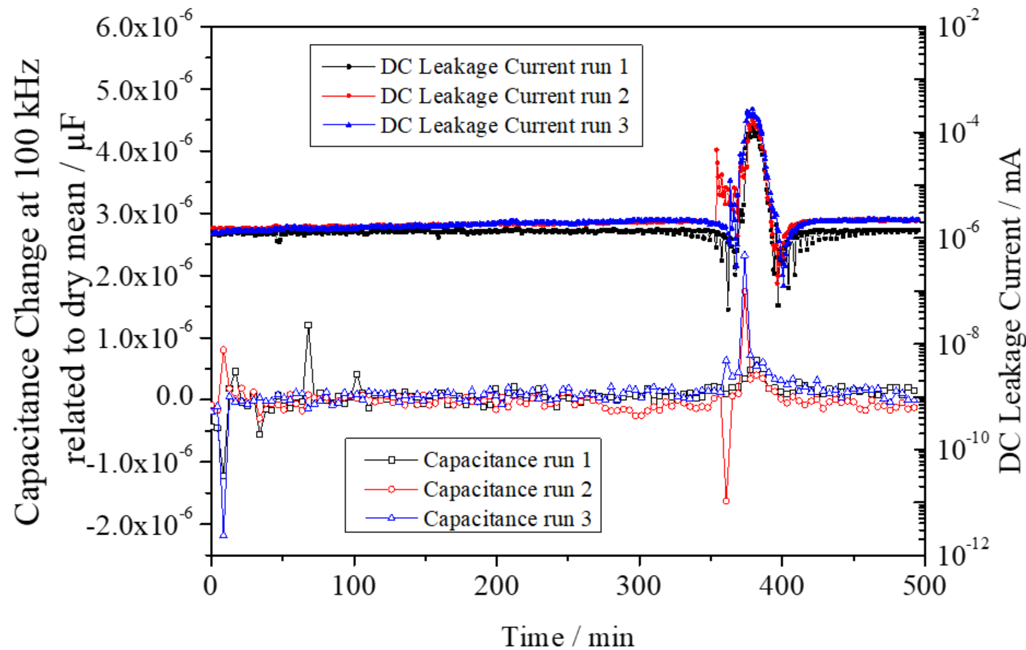


Figure 9.9: EIS results displayed in form of a Capacitance Change at 100 kHz related to the mean value of the pattern in dry condition. DC results displayed in form of Leakage Current data.

Analysis and Discussion

The findings based on the experiments demonstrate the potential of EIS in assessing the water layer needed for ECM non-destructively. Both resistive as well as capacitive changes in system properties can be used for evaluation.

In measurements conducted with the T-shaped patterns on FR-4, the intermittent EIS-sequences deliver more comprehensive information than the DC. This provides a better understanding of the dendrite occurrence. The capacitive changes throughout the climatic profile deliver information on the detailed humidity state of the system. This way, differences in run 1 and run 2 of the experiment can be revealed. In run 1, the *Cp* value stays below the dry state baseline for a certain time span. This can even suggest that residual humidity present in the laminate in the high humidity ambient is driven out in this time frame. A respective amount of humidity is needed to condense on the sample during the second temperature peak, as laminate pores need to be filled first and then condensation islands need to connect into a film. Hence, more time is required for the dewing process before dendrites can form. Comparing with the *Cp* in run 02 it becomes apparent that a return to a dry value does not occur during the whole profile. This indicates that

there is water present on the surface the whole time, potentially at least in the form of capillary condensed water. Respectively, the harsher condensation established in the second peak is already facilitated. It is conceivable that electrochemical reactions like Sn-oxidation can take place already in an earlier stage compared to the run 01 specimen. Electrochemical migration of Sn and Sn based compounds under electrolyte layers has been subject of different literature studies [5,39,40]. It is stated that a moisture layer of a few monolayers is sufficient to initiate the corrosion process. The process starts with the oxidation of Sn at the anode, where it is hydrolyzed. The chemically neutral tin hydroxide tends to precipitate. However, if the thin water bridge is established from anode to cathode and the alkaline environment of the cathode spreads far enough into the layer, Sn-OH-complexes can form and eventually be reduced at the cathode, starting dendrite growth. For run 02 with continuously present humidity on the surface, it is likely that part of this process chain can occur easier compared to run 01. Thus, from the EIS data, it can be assumed that this is the reason for earlier dendrite growth. As this information cannot be resolved from the DC testing, the EIS measurement shows a clear advantage for understanding the failure occurrence.

With regard to the testing performed on LTCC patterns, a comparison of EIS and DC shows that the increased humidity level on the surface is mirrored in both techniques. Unlike the tests performed on PCB laminate, the changes in EIS signal however occur simultaneously with the DC. No premature information is provided by the EIS measurement. This can be attributed to the different process of water level buildup on the LTCC surface compared to the FR-4 and the detection possibility relating thereto. FR-4 and LTCC surface show fundamental differences in their properties. In Figure 9.10a) and b), SEM micrographs for FR-4 and LTCC surface are shown. The structure the epoxy resin FR-4 laminate is clearly visible. The topography shows a mesh network with large pores that are up to several micrometer in their dimension. In contrast, the LTCC surface shows a very much non-porous structure. The substrates also differ in wettability. In Figure 9.10c) water contact angle measurements for both surfaces are displayed. The contact angle for FR-4 has a mean value of 112 °, for the LTCC substrate it is 54 °. Compared to FR-4, the LTCC sample exhibits a somewhat higher wettability.

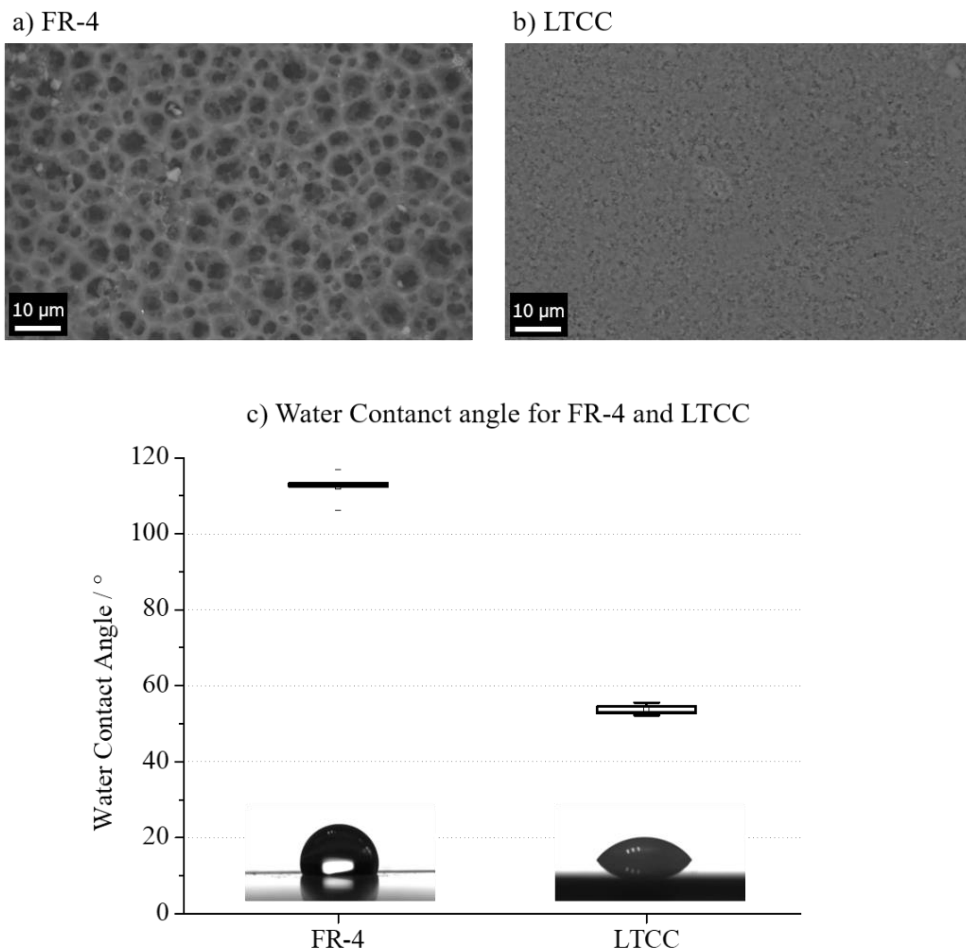


Figure 9.10: SEM micrographs of FR-4 (a) and LTCC (b) surfaces. Water contact angle for FR-4 and LTCC surface. Data for mean values and deviation is based on each five measurements (c).

The FR-4 laminate is known for doubling moisture ingress at an ambient humidity as low as 40-60 %rH and temperature of 40 °C [41]. For non-absorbing ceramic surfaces, relative humidity in this range has been shown to result in water adsorption of a few monolayers instead [42]. These differences affect the water interaction of the surfaces in a high humidity environment and with this the progression of EIS and DC measurement values.

The large pores in the FR-4 base material result in the actual internal surface of the substrate being much larger than that of the LTCC. Therefore, in case of FR-4, first steps in condensate formation need to be considered as capillary condensation process [43]. This means that once single water molecules have formed a monolayer configuration (Figure 9.11a), (i)-(ii)), subsequent humidity interaction results in allocation of less firmly bound water molecules that build up multilayers above the monolayers in the surface irregularities (Figure 9.11a), (iii)-(iv)). The condensed water is governed by suction pressure in

pores. The moisture sorption process on the LTCC substrate is based on a physisorption process, transferring from monolayer to multilayer formation (Figure 9.11b)). This buildup is possible due to the highly planar surface, allowing a linear water concentration profile across the whole area and subsequently a uniform growth.

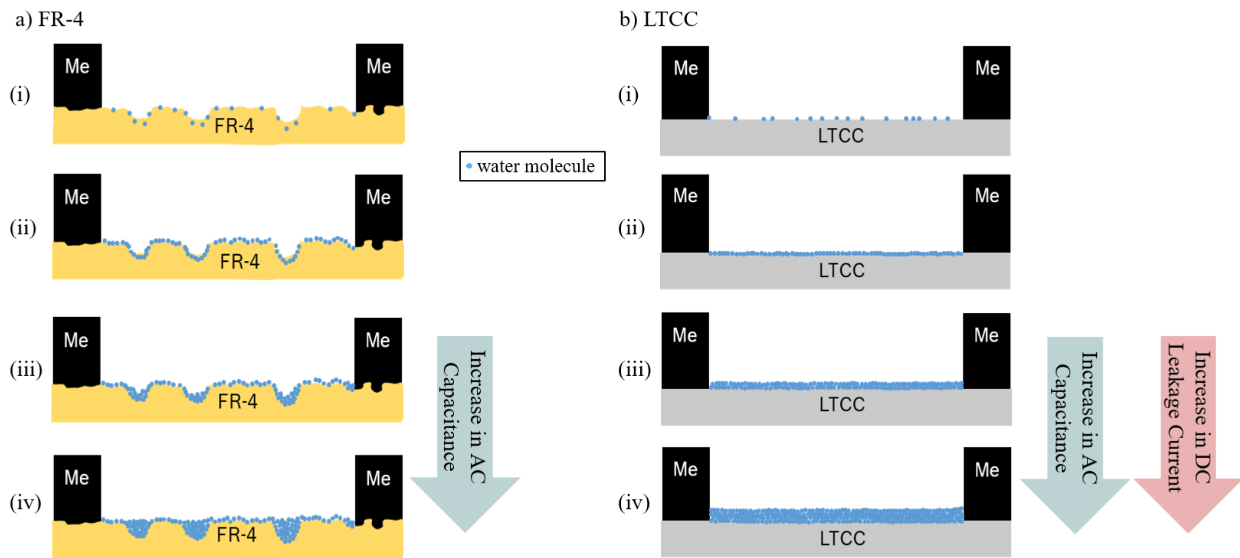


Figure 9.11: Model concept of the initial steps of water condensation on porous FR-4 substrate (a) and comparably non-porous LTCC substrate (b) along with AC and DC detectability.

The pore filling of the laminate supposedly governs the increase in AC capacitance for the FR-4 substrate. This results in a change of the capacitive character of the laminate with adsorbed water in between the comb patterns due to overall permittivity increase. Assuming an RC-parallel circuit, as has been done for elaboration of the presented results, the complex impedance can be used to comprehend how in terms of water film buildup on the PCB surface, especially capacitance parameters deliver valuable information. Equation 9.1 shows the complex impedance Z for an RC-parallel circuit with resistance R and capacitive reactance X_C. With Equation 9.2 and Equation 9.3, the impedance can be expressed according to Equation 9.4, with frequency f, permittivity of the vacuum ε_0, relative permittivity ε_r, active electrode area A, specific resistance ρ and electrode distance d.

$$Z = R + jX_C \quad \text{Equation 9.1}$$

$$X_C = \frac{-1}{2\pi f \varepsilon_0 \varepsilon_r \frac{A}{d}} \quad \text{Equation 9.2}$$

$$R = \rho \frac{d}{A}$$ Equation 9.3

$$Z = \sqrt{\left(\rho \frac{d}{A}\right)^2 + \left(\frac{-d}{2\pi f \varepsilon_0 \varepsilon_r A}\right)^2}$$ Equation 9.4

In the first stages of dew formation, on the FR-4 laminate, pores are filled. Thus, the first changes in overall impedance are mirrored in changing relative permittivity. In dry state, the expression is governed primarily by $\varepsilon_{FR-4} = 2.8\text{-}4.6$. With commencing condensation, water impact on overall permittivity needs to be regarded as well ($\varepsilon_{water} = 79.5$) [44]. This can already be detected by EIS as an increase in AC-capacitance (Figure 9.11a), (iii)-(iv)). As individual droplets create an interconnecting layer, which is the case very early on for the LTCC substrate, both EIS and DC tests detect this state (Figure 9.11b), (iii)-(iv)). As the layer builds up further and the impact of water permittivity increases, this is gradually identified by the capacitance equivalent used in EIS, up to a point where the overall capacitance is only determined by ε_{water} and therefore further increased. The DC testing however fails to clearly distinguish the water layer growing in height. As the water film connects the electrode gap, the overall impedance is strongly affected by the specific resistance ρ in Equation 9.3, now being the resistance of the water film. This way, the electrical properties of the water film are also mirrored in the measurement. Thus, EIS has detailed humidity sensing capability. It is able to distinguish the first steps of water adsorption, water droplets in between electrodes, their merging into an interconnected film, film growth and the electrolytic properties of the film.

In the light of the results in their entirety, including different design elements and surface materials, it is apparent that EIS delivers comprehensive insights on the water amount present in between the contacts. This is true for both condensation testing as well as in the context of transient climatic conditions during cyclic profiles. Gradual humidity buildup as well as the transition points into an ECM-critical water film can be detected non-destructively by capacitive or resistive parameters. However, a detailed knowledge on the surface characteristics is important to actually assess the imposed criticality by both EIS and well as DC measurements. In the case of the LTCC samples, water adsorption or pore condensation are of no relevance. Instead, monomolecular layers of water build up once ambient humidity increases. This is mirrored in AC and DC at the same time. The signal change in the DC is even more pronounced, presumably because electrical conduction via the water layer is possible for very few molecular layers already. Thus, even though the AC does not show considerable changes, in terms leak current increase, this state is already critical. Therefore, EIS cannot be considered a universal remedy in assessing humidity criticality without caution. Nevertheless, EIS has proven to deliver predictive information on ECM-critical water loads for laminate substrates. Independent of design parameters like gap size or FR-4 or solder mask surface,

condensate formation can be traced and transition towards a gap-bridging film can be determined. EIS should therefore be regarded as part of an evaluation chain, in which it can deliver in depth comprehension on the humidity present in a system. Combined approaches of EIS and DC measurements, along with comprehensive understanding of the surface structure should be merged in further testing to allow a holistic evaluation of critical humidity.

IV. PART 3: EIS FOR PREDICTING IMPEDING FAILURE ON AN ASSEMBLED BOARD WITH COMPONENTS

Studies using EIS and DC methods described earlier were focused on simple conductor structures. Although, during the design stage of electronics, a PCBA design element is tested by such patterns, next level testing is carried out with an assembled board with actual or dummy components. At this point, this also includes testing of processability of solder materials in terms of reliable solder joint formation. As the assembled board reliability is a crucial factor in development, it is important to understand whether EIS can also be used in this case instead of DC methods.

The product development process for automotive electronics involves general reliability verification, which includes validation of subsystems like specific materials or components. Once basic testing is completed, released materials can be integrated into a larger platform. Testing climatic reliability is supposed to generously cover highly demanding operating conditions like extreme temperature (–40 °C – 125 °C), or mechanical stresses like vibration. Electronic modules are tested for stability in repeated active and passive thermal cycles and assembly approaches [45–47]. For electrical testing in these climates, the SIR test is widely used. Qualification of materials or modules are performed accordingly, based on different standards, which regulate the SIR test conditions [11,48]. The SIR method has a long history of application and provides advantages like fast and easy technical implementation and the possibility to test various design elements. However, associated problems are also frequently reported. A common problem is the detection of pseudo failures that show a corrosion critical SIR-value, even though the test system is not in an actual critical state. The reaching of such values can be simply attributed to contamination particles like fibers on the test patterns [28]. Accordingly, simply relying on SIR-thresholds during testing is insufficient in order to assess reliability of a test pattern. Extensive post-testing analysis is often necessary, as the SIR test cannot provide a comprehensive cause-effect relationship. Some studies also question the general suitability of SIR tests to detect humidity induced failure modes [49]. Also, assessment of cleanliness level, hence a valuation of residues that remain on a board after soldering, is reported to be limited by SIR measurements [50]. In the context of Surface Mount Device (SMD) technology, critical flux residues remaining on the board after soldering are known to severely affect reliability. The flux residue's significance in relation to

corrosive processes has been evaluated in various studies. The presence of ions in the electrolyte affects ECM, as has been shown for copper electrodes in a chloride ion-containing electrolyte [51]. The effect of flux residue on the humidity related failure issues has been investigated under common PCBA qualification conditions (40 °C/93 %rH and 85 °C/85 %rH), but also during gradual humidity ramp-ups of up to 99 %rH [36,52–54]. Fundamentally, the possibility for ECM is enhanced by the presence of ionic contamination. Especially the weak organic acids (WOAs), used in no-clean flux systems, are reported to be critical [36,55]. Use of no-clean flux systems involves careful consideration of aspects like utilization of proven materials, on- and offline contamination monitoring and a well-design manufacturing process [56]. However, investigations on solder profiles show that the assembly process can already be problematic, as for example temperature on a PCB during wave soldering does not always reach the intended values in all areas of a board [52]. The remains of only partially activated flux residues on a board can be a considerable ECM risk for the setup. Specifically trapped under low standoff-devices, it is problematic in terms of corrosion [57]. Upon exposure to humidity, these residues open up due to hydrolysis, releasing ionic residues below the component. Their hygroscopic character additionally enables the formation of a water film even if humidity levels or temperatures are lower than that required for condensation.

Due to these issues, it is important to have measurement approaches that are able to display the criticality and detect residue-assisted water film formation in early stages. In the presented experiment, EIS and DC technique were used to perform measurements on a PCBA with assembled BGA components. These components are considered particularly critical, as their solder balls are extensively covered. The component acts as lid, hampering flux outgassing during soldering. This results in the presence of concealed reflow flux residue under the component. Water bridge formation below the BGAs is very critical, as the covering impact of the components also affects re-evaporation of the dew. The aim of the tests described below is to display how EIS testing can be used to uncover critical states for more complex PCBA setups. The greater humidity detection capabilities of the EIS method compared to DC testing is debated in this context as well. If the EIS is able to counteract pseudo-failure problems of the SIR test or the unsatisfactory information on cause-effect relationship, the method can be used as a substitute or complimentary to conventional DC testing.

Experiments with assembled boards

The DC Leakage Current and intermittent EIS measurements were performed on the circuitry as shown in Figure 9.12 with SMD-soldered BGAs. Two BGAs were connected to one measurement channel (Figure 9.12a)). As a reference, a board without BGAs was included in the test (Figure 9.12b)). The circuit of the 16 x 16 solder pads was implemented on the board by an interdigital comb circuitry with eight arms each

Figure 9.12c)). The base laminate was made of standard FR-4. The solder material used was a standard SnAgCu based SMD no-clean solder paste for automotive. The solder balls had a pitch distance of 300 µm. The stand-off of the components after reflow soldering was approx. 150 µm. The board with SIR patterns without BGAs was made of Sn without any solder paste. The boards were not cleaned after manufacturing. Two boards with assembled BGAs were used for DC Leakage Current with intermittent EIS measurement. One board without solder and BGAs was used as reference testing.

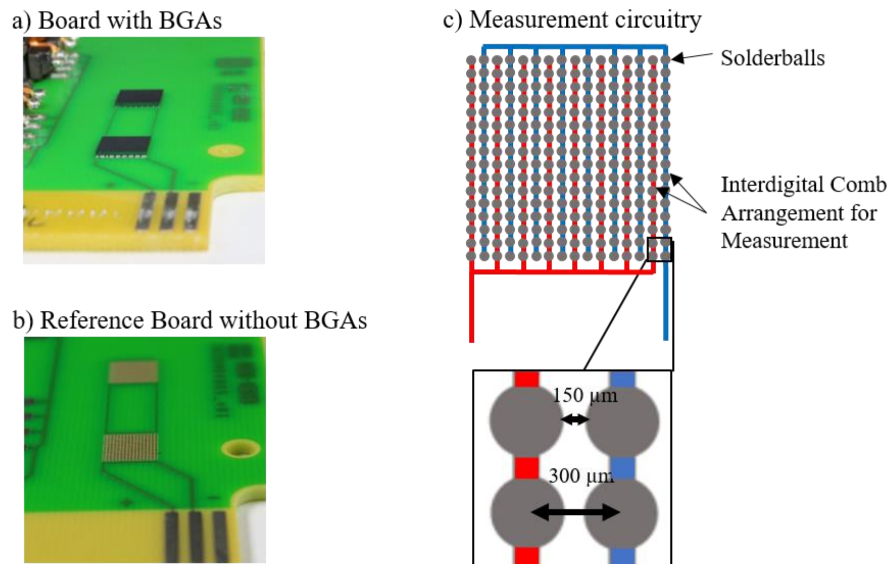


Figure 9.12: Photographs of test board with assembled BGAs (a) and Reference Board without BGAs (b). The measurement circuit based on an interdigital comb arrangement is schematically displayed in c) Solder balls with 300 µm pitch distance are shown in grey, the two Sn-lines representing the electrodes are displayed in blue and red.

For the electrochemical measurements of the three boards, a potentiostat system (VSP, BioLogic Science Instruments, France) enabling both measurement modes was used. As previously described, for correlation of EIS and DC values, the method were performed in a repetitive manner. They were alternated with 30 s wait periods in between. The EIS-sequence was carried out for five cycles in a frequency range from 100 mHz – 100 kHz, and the corresponding duration of a sequence was nine minutes. During a DC-sequence, a potential of 10 V was applied and Leakage Current was recorded. The duration of a DC sequence was 15 minutes. By using the intermittent mode, EIS measurements were able to detect the humidity status on the board. Intermittent DC testing with its ECM-promoting characteristics demonstrated whether the absorbed humidity was sufficient to enable dendrite formation.

To impose critical climatic conditions on the samples, a 175 hours heat-damp cyclic test according to IEC 60068-3-4 was performed (Figure 9.13). Temperature was cycled six times between 25 °C and 55 °C. Ramp time was 3 hours; temperature was kept steady at each 25 °C and 55 °C for 7 hours. The relative

humidity during cycling was set to 96 %rH. The test was carried out in an "Espec PL-3 J" test chamber (ESPEC Corp., Japan). To increase the severity of the testing as in actual application, the boards were fixed onto an aluminum block of 2 cm thickness. By means of this heat sink, water condensation on the PCBA surface was enhanced.

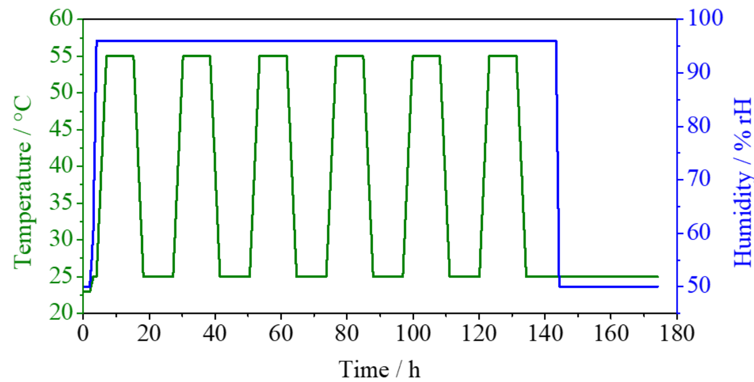


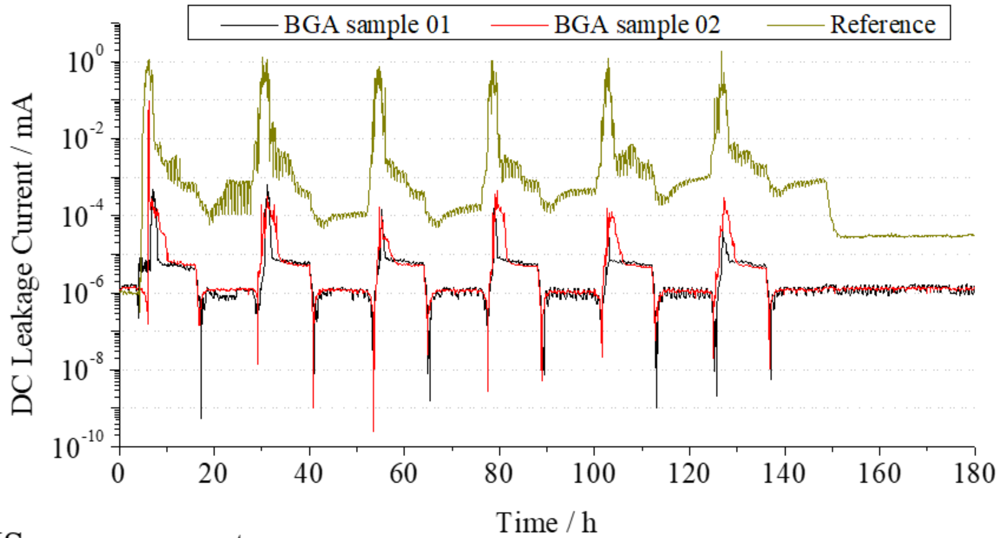
Figure 9.13: Climatic Profile imposed on the samples during heat-damp cyclic test.

For the three measured boards, DC Leakage Current and Capacitance data at 30 kHz have been chosen to evaluate. The 30 kHz-frequency was chosen as a suitable EIS parameter based on the above described facts that the capacitive properties of the system are more dominant in the higher frequency range. For the whole course of the climatic profile, Leakage Current and Capacitance for both of the patterns with BGAs as well as the reference pattern are shown in Figure 9.14. Capacitance values are standardized to a mean dry value in order to show the deviation from dry state for all patterns. This provides a uniform scaling of capacitance values for all measurement channels, circumventing the initially different capacitance values for patterns with and without BGAs. In order to do so, for each pattern, the mean dry state capacitance was obtained from five EIS cycles before the climatic profile was initiated. The respective values were each subtracted from the proceeding capacitance values during cycling.

Figure 9.14a) shows the leak current results from the DC. The impact of humidity adsorption to the boards due to temperature cycling is clearly visible. Current increases once temperature is ramped up to 55 °C and decrease upon ramp down to 25 °C. Capacitance values (Figure 9.14b)) from the patterns show similar results with increasing capacitance when the temperature is ramped to 55 °C, while it decreases to normal values at 25 °C. Considering the Leakage Current, a clear distinction can be made for the samples with BGAs and the reference structure without component covering. Starting out at approx. 10^{-6} mA, the reference current (green) already reaches 10^{0} mA after 6 hours during the first cycle. In the ramp down step, it decreases once more, though not back to its initial value as it remains in the order of 10^{-4} mA. This is also the case for the following cycles. The current follows the temperature ramp up, but it stays at 10^{-4} mA upon

ramp down to 25 °C. The current value for the reference structure current does not return to the initial value at the end of test. After 152 hours, it stabilizes at 3 x 10^{-5} mA, indicating remaining dendrite formation between the interdigitated pattern of the open comb structure.

a) DC measurement



b) EIS measurement

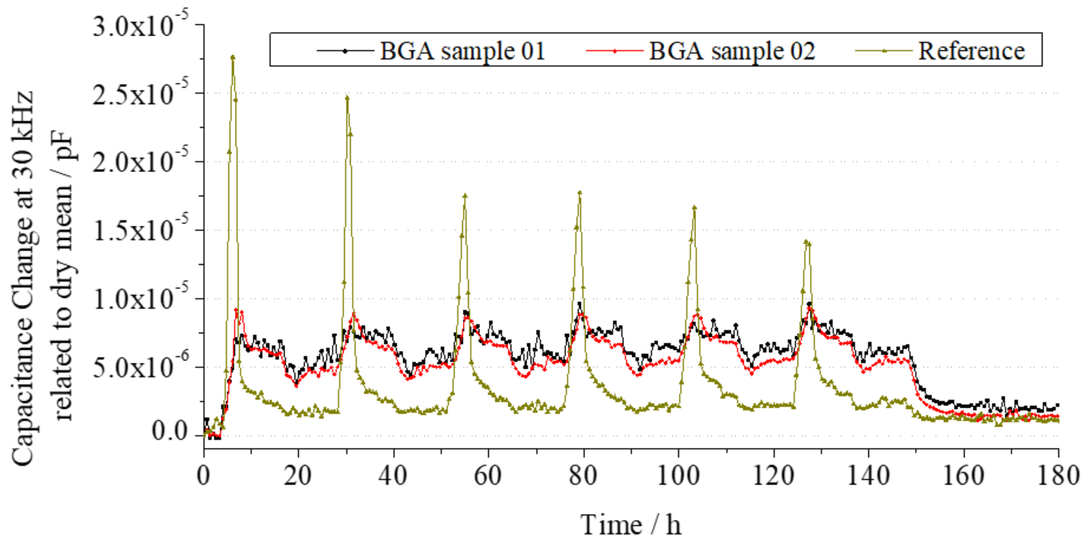


Figure 9.14: DC Leakage Current data during climatic profile for the BGA samples and the reference pattern (a). EIS data displayed as Capacitance Change related to dry mean value for the BGA samples and the Reference pattern (b).

To present the differences between EIS and DC measurement in detail, a closer inspection of beginning and end of the climatic profile was deduce from the above figure and shown in Figure 9.15 for the first 30 hours of the measuring profile.

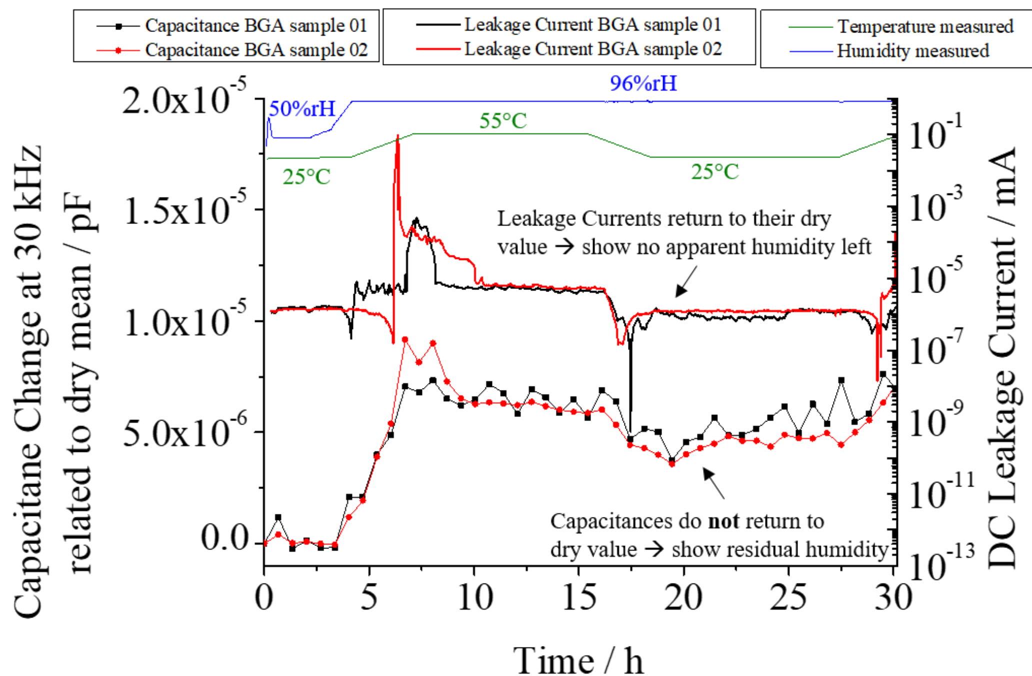


Figure 9.15: Signal progression of measured climatic profile, DC Leakage Current and intermittently measured EIS-Capacitance at 30 kHz related to dry mean from 0-30 hours into testing.

The currents show a major increase upon temperature ramp up. However, they only reach a maximum of 4.8 x 10^{-4} mA (BGA sample 01, black) and 9 x 10^{-2} mA (BGA sample 02, red). After this initial increase, both curves drop to a level of approx. 5 x 10^{-5} mA after 10 hours into the profile. This range is maintained until the current drops back to the initial range of 10^{-6} mA once temperature has reached 25 °C again after 18 hours. Currents remain stable until the second temperature cycle starts after approx. 30 hours. During each of the following five temperature cycles, the curve progressions are in principle analogue, with both sample remaining in the same maximum peak area of 10^{-4} mA (Figure 9.14). Regarding the Capacitance change related to dry mean, the reference structure (green) in the EIS shows a significant increase during the first temperature peak as well. It reaches a value of 2.75 x 10^{-5} pF, however it quickly drops and has stabilized at 2 x 10^{-5} pF after 20 hours. In the case of patterns covered with the SMD components, the course of capacitance deviates from the reference structure in a way that values reached are generally not as high. However, they also do not drop significantly anymore when temperature returns to 25 °C. For both BGA sample 01 and 02 (black and red), in the first peak maximum values of 7 x 10^{-6} pF (sample 01) and 9 x 10^{-6} pF (sample 02) are reached. Even though the values drop again during temperature ramp down, they do not fall much below 5 x 10^{-6} pF anymore (Figure 9.15).

At the end of test when temperature has returned to 25 °C and humidity is ramped to 50 %rH, EIS and DC also vary in their output signal. The last part of the current and capacitance profile for the BGA patterns is

shown in detail in Figure 9.16. Looking at the Leakage Currents, they have already returned to their initial dry state value in the range of 10^{-6} mA, even before humidity is at 50 %rH. The Capacitance however shows a different picture: Until *t* = 148 hours, it is still at level of approx. 6 x 10^{-6} pF. Only after about 160 hours, the values for both test boards stabilize in the 2 x 10^{-6} pF-range. Thus, even at the end of test (at 25 °C/50 %rH)), they lay above their initial dry values (also 25 °C/50 %rH).

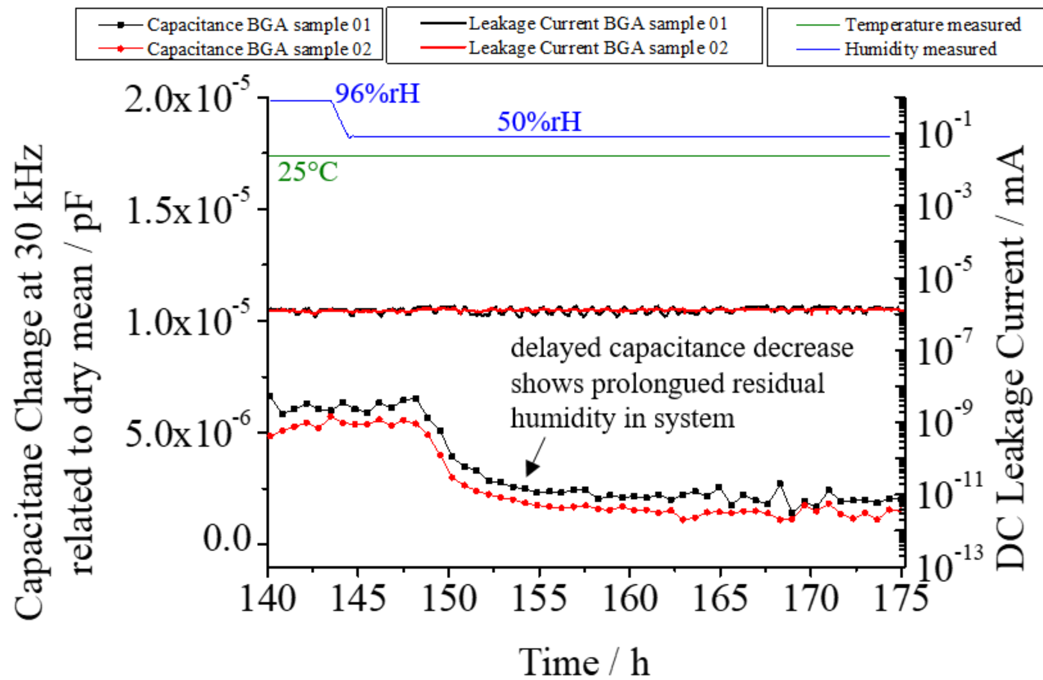


Figure 9.16: Signal progression of measured climatic profile, DC Leakage Current and intermittently measured EIS-Capacitance at 30 kHz related to dry mean from 140 – 175 hours of testing.

Analysis and Discussion

Comparability of patterns with BGAs and the reference structure in terms of measurement signal comparison is hampered by the fact that the DC indicates that the reference pattern has already grown dendrites in the first cycle. Extraction of the sample after measurement also confirmed severe dendrite formation. It is therefore not conspicuous that Leakage Current and Capacitance did not return to starting values at the end of test. In case of the samples with mounted BGAs, Leakage Current returns to the initial value of 1 x 10^{-6} mA, indicating no dendrite formation. Cross-sectional inspection of the specimen after testing did not show any dendrites. It must therefore be assumed that the capacitance values not returning to the initial baseline at the end of test is attributed to delayed humidity withdrawal below the components. Also, the fact that during the separate six cycles the capacitance has never fully decreased again in the 25 °C steps (Figure 9.14), is presumably due to this circumstance. When comparing the DC and the EIS at distinct

points during the climatic test, the DC does not indicate extra humidity in the system, while the EIS clearly does (c.f. Figure 9.15 after 17 hours). In both signals of EIS and DC shown in Figure 9.14, a step-wise reduction in humidity during the evaporation (temperature ramp back from 55 °C to 25 °C) seems apparent. In the DC, a strong value increase occurs during temperature ramp up which is followed by a fast decline to a value range that is held for a few hours (also seen in detail in Figure 9.15, 10-16 hours). The EIS capacitance roughly follows this scheme. However, while the DC fully decreases again upon ramp down, the capacitance only decreases down to a slightly lower level. It is conceivable, that with the fall of the DC current, the connection of a thin water film across the tracks below the component is ruptured. Still, there is non-evaporated water present, which is detectable by EIS. It can be assumed that hygroscopic residues from the soldering process are located on the board below the components. Beside the difficulty for the humidity to evaporate due to the enclosing characteristic of the BGA component, these residues can additionally hamper humidity withdrawal. The fact that evaporation times of water droplets change with degree of purity has been stated in different studies [58,59]. In the case of ionic contamination, such as NaCl, it is assumed that the electrostatic interactions of oxygen atoms and Na^+-ions on the one hand and hydrogen and Cl^- on the other hand entails a strength higher than that of a pure water film. This results in an impeded evaporation. In a thermodynamic consideration, a higher ion concentration in the water reduces the water vapor pressure, which again reduces the evaporation rate [60]. The residues from soldering processes are acid based, primarily weak organic acids (WOAs) come to use. They tend to absorb moisture due to their polar functional groups and retain it even under changing climatic conditions [61,62]. Consequently, they are associated with a greater risk in the context of PCB’s climatic reliability [54]. With regard to ECM criticality, several risk factors play a role in the tested setup: Bad outgassing of flux residues below the components lead to enforced condensation once water vapor gets below the components. Electric conductivity of the formed water layer is enhanced due to ionic character of the flux residues. Furthermore, water evaporation is hampered by the hygroscopicity of the flux residues, in addition to the covering function of the component. While the DC is not able to replicate this criticality, the EIS clearly indicates the actual humidity status below the BGAs.

EIS also shows in detail another consequence of the repeated temperature cycling. Looking at the Capacitance values for both BGA-samples over the course of the whole climatic profile (Figure 9.14), a slight stepwise increase of the values reached during the 25 °C-sequences can be recognized. This is believed to be due to a pumping effect, meaning that due to no full outgassing, more humidity is accumulated below the component with each temperature cycle. This effect has already been observed as response of enclosures of electronics with relation to cyclic climatic conditions [63]. It was also demonstrated that the transition towards enabling closed water film formation is sudden. This is why even

though no dendritic failures occurred in the conducted tests, it can clearly be seen that the EIS method is beneficial for early non-destructive assessment of moisture status below critical components. The results look promising in terms of predicting humidity induced failures on whole PCBA assemblies. The indicated possibilities of EIS being able to detect critical states that the DC cannot identify should therefore be a topic for future testing.

V. OVERALL DISCUSSION ON EIS COMPARED TO DC APPRAOCHES

Overall, this paper shows that the EIS technique can be effectively used as a complementary method for evaluating humidity effects on PCBA together with or without the DC methods depending on the requirement. The use of EIS can provide more detailed information on the water film buildup, while one substrate can be used for multiple tests.

With regard to general water film buildup detection, the process can be displayed by the use of various EIS parameters. Fundamentally, a broad band of frequency is able to display proceeding condensation, while the best frequency range for detection can be application dependent. Likewise, depending on substrate material and electrode geometry, different frequencies can be suitable for evaluation. However, based on the extensive studies performed, some general conclusions can be made for the test patterns and condensation conditions presented in this paper. It was determined that from 1 - 10 kHz, the biggest impedance and phase shift changes occur in early stage adsorption. Merging of droplets into a film is reflected more in 10 - 100 kHz. One of the greatest advantages of EIS is the possibility to distinguish different processes and process kinetics by employing a broad frequency range. Likewise, this is also one of the disadvantages compared to conventional approaches like the SIR. In relation to simple DC testing, when employing EIS, more basic knowledge of the system is needed for the determination of test specifications.

However, the results clearly reveal that the EIS is extremely valuable as both resistive and capacitive system properties can be obtained from one measurement. The results presented in this work show that changes in capacitance can be related to humidity uptake and initial water layer buildup. Formation of a conductive bridge, its increase in height and electrolytic properties, for example affected by ionic contamination, can be represented by resistance changes. Accordingly, the method provides extensive information on the water film buildup and relation of a possible ECM-onset.

When considering EIS as a method to replace the DC approach, the greatest problem is the aim for a universal threshold value in large scale testing. The determination of one critical value (like 10^8 Ohm in SIR) for all kinds of sample setups with EIS is not yet clarified. The first promising findings indicate that

for different pattern geometries, an ECM-critical water film can be described with a universal impedance value (≦ 2 x 10^4 Ohm for 68 kHz frequency), however more extensive studies with different PCB designs are required. While EIS can be used for predicting the possibility of failure under a DC condition by following the water film buildup, the exact time to failure needs to be determined using the DC method as the application conditions for the PCBA is DC. However, EIS can still be highly beneficial as many structures can be tested using EIS, and the selected critical ones can then be tested using DC.

VI. OVERALL SUMMARY

This work presents a holistic overview of different studies in the context of implementing Electrochemical Impedance Spectroscopy for assessment of humidity robustness of electronics. The compilation of results considers discriminatory aspects. The main benefits of the EIS technique are demonstrated according to existing literature and supported by further studies. Especially noteworthy is the fact that EIS is a method that is non-destructive to the specimen, meaning tests in different (climatic) scenarios can be repeated with one sample. It was also shown that critical humidity states can be detected prior to significant changes in conventional DC testing methods and prior to ECM failures. The fact that using EIS eliminates the need to wait for a DC-failure is extremely valuable in the assessment of a critical humidity status. EIS has also shown to be more sensitive in different testing scenarios and to be able to deliver more comprehensive information on the presence and properties of electrolytes. The results also clearly demonstrate how valuable EIS can be for PCBA testing with critical components and contamination impact. The method has proven to be more advantageous than the DC measurements when wanting to fully comprehend the impact of climatic conditions. Evaluation of capacitive and resistive system properties allows the definition of ECM-critical threshold values like the 68 kHz EIS-impedance of ≦ 2 x 10^4 Ohm for different SIR patterns on standard laminate. Additionally, detailed analysis of parameters like parallel capacitance or more extensive electrical equivalent circuits can provide more in-depth information on electrolyte properties. According to this, EIS results could be used to predict ECM-critical conditions. Based upon understanding all influencing factors, a comparison of EIS and DC methods and consequently the consideration of EIS as an alternative improved validation method can be aimed for in the future.

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10. GENERAL DISCUSSION

In the light of the presented studies, this chapter contains a short discussion on the findings established in this PhD work. The results clearly show the importance of understanding condensation in water film buildup in order to avoid possible failure mechanisms like ECM. Results from the measurements are particularly important in connection with the early stages of product development, when layouts are designed, materials are tested, design elements are validated or manufacturing and cleaning procedures are specified.

Accordingly, the implementation of EIS for reliability assessment implicates various chances and opportunities. In an industry environment, the method and its potential applications still have an innovative and future oriented character; however, in academia, EIS is already a well-established approach. The EIS signal provides the means for characterization of water film properties and thus enables determination of various factors important for humidity related testing: water film thickness, residue content and bridging behavior can be evaluated non-destructively. These properties can be correlated with local temperature and humidity information and be fed into simulation models for condensation. In addition, the data can be related to the occurrence of a failure mode in the case of DC signal application. As the EIS approach does not provoke the failure itself, testing can be repeated multiple times on just one specimen in different conditions. In doing so, not only the water film formation but also evaporation processes can be studied in a highly reliable manner. Also, statistical relevance of testing can be achieved with less effort, time and cost compared to conventional DC SIR testing that requires new samples for each test case due to its corrosion provoking character. EIS could thus overcome the intensive experimental approach that is required for SIR testing.

EIS has been demonstrated to be very sensitive towards smallest humidity changes in a PCBA setup. The experiments in this work show that a critical humidity level is measurable prior to dendrite growth upon DC. Moreover, not only condensation on the surface, but also humidity absorption can be detected. This can enable measurement that goes beyond dendrite growth assessment. Also, the change in properties of coatings or base materials can be studied and EIS has potential use for such material degradation measurements. Overall, the humidity sensitivity can serve the purpose of a deeper understanding of cause-effect relationships than possible with DC testing. The SIR approach partially shows failures only in late stages of product design and fails to discover potentially critical materials or conditions prior to platform testing. The results in this work generated by the EIS method, especially for assembled boards, show the potential of early stages discovering of quality issues. This way, EIS can be used as tool for predictive diagnostic on component level and on system level. Unlike the DC method, which detects primarily the

failure like a “sudden death”, EIS can provide progressive information on the water layer buildup and how its electrical behavior contributes to the failure under DC conditions.

The pursuit of using EIS for humidity related reliability testing requires dealing with some risks that need to be further considered. One of the most important factors is the question for threshold values that indicate a test failure, hence an ECM-risk. Common DC SIR testing sets threshold values like 10^8 Ohm that specify a failure once the value is undercut, independent of materials, design elements or layouts. For the EIS approach, it is not clarified whether a similar threshold value, valid for a variety of sample patterns can be found. EIS is able to give information on water film properties on the surface, however a steady potential application is needed to calibrate whether a distinct water film enables ECM. As for applicability of the method in material or product release, EIS will continue competing with the DC testing, which comes with the advantage of having a straight forward correlation between measurement signal (as in dropping below an SIR limit) and failure mode (as in short circuits due to corrosion products). EIS is certainly still more sensitive towards humidity changes in a PCBA system under test. However, the sensitivity of the method and the impact of different variables like material and design on the measurement data need to be understood in detail to make the approach useful for large scale testing.

11. GENERAL CONCLUSION

The goal of this work was to establish a correlation between conventional DC leakage current testing and water film information from EIS measurement. In doing so, an allocation of an ECM-critical state and evaluation of influencing factors by EIS was aimed for. The fact that the technique does not harm the samples enables testing in different conditions with just one board. Overall, all of the conducted experiments confirm that EIS brings large value add for various testing scenarios. The following points can be concluded in this context.

1. It was shown that water buildup on the PCB surface can be detected non-destructively by EIS on different specimens in terms of materials and designs for various temperature and rH conditions. In-situ monitoring of the water layer formation was performed in order to classify the EIS values. A drop in impedance and a shift in phase angle towards zero values can retrace the gradual condensation process. Frequencies between 1 kHz and 100 kHz show this characteristic progression, with the largest value delta from dry to wet in the higher frequency range. Also, considering the specimen an RC parallel circuit and evaluating the parallel capacitance fit displays the water film formation from early stages on.

2. The DC leakage current development during condensation, ECM and eventual dendrite formation was groupable into three ranges: (i) for a dry surface state, currents remain below 1×10^{-4} mA. (ii) in condensation regime, currents between 1×10^{-4} mA – 1×10^{-2} mA are obtained and (iii) current magnitudes exceeding 1×10^{-2} mA indicate dendrite shorting. Temporal conditions of the regimes strongly depend on the electrode gap size (e.g. 300 µm gap condensation transition regime is more than twice as long as 100 µm gap). The transition from condensation range up to high leak currents due to the conducting dendrite is not progressively detectable with DC. Instead, a sudden jump occurs from some value in the condensation range the moment the dendrite bridges the gap.

3. Intermittent measurement of EIS and DC in alternating manner allow a good correlation of water film status and dendrite occurrence. EIS was able to gradually measure the step-by-step increasing water load. In temporal consideration, the condensation was displayed at the same time as in the DC for most experiment settings. For slow-condensing conditions, dew formation was even detected earlier by EIS compared to DC testing. This demonstrates the advantage of the EIS methodology's sensitivity towards changes in dielectric system properties in early stage water adsorption.

4. This way, critical EIS values traceable to distinct water bridging levels allowed the assessment of an ECM-critical test board state. For non-contaminated samples, it was evaluated that independent of comb pattern gap size and surface material, an EIS-impedance of $\leq 2 \times 10^4$ Ohm at 68 kHz signifies an

ECM critical water bridge between the conductors. The prominent changes in the EIS signal occur prior to the DC failure enable it to forecast ECM non-destructively.

5. Gravimetric measurements in different condensation regimes showed that the water layer thickness that is needed for the formation of gap-bridging dendrites can be associated with “bulk water” layer thickness.

6. The localization of corrosion hot spots plays a key role in assessing climatic reliability of PCBA setups. Among the influencing factors, the surface temperature distribution, affecting local undercutting of the dew point, is important to consider. By means of AC impedance measurement, the impact of a non-homogenous temperature distribution, enforced by a heat-radiating component can be evaluated. This allows the non-destructive determination of ECM-safe areas on a board with mounted components. For a test case it was shown that an SMT-diode powered with 0.4 A prevents ECM-critical water bridge formation across 100 µm gaps of up to 13.35 mm surrounding radius.

7. Local accumulation of contaminants strongly affects condensation and enhances the ECM risk. Time Domain Reflectometry as non-destructive impedance technique has proven to detect enhanced condensation at flux residue spots on a PCB surface along a 90 mm long copper track.

8. EIS was demonstrated to be highly sensitive towards humidity changes in a test system. On boards with mounted BGAs of high criticality due to narrow distances and covered solder joints, residual humidity below the low-standoff component was detectable by capacitive changes in the EIS signal. The DC technique failed to sense these humidity conditions. Accordingly, EIS shows the potential of being used for predictive assessment of weak points, for example in terms of layout or climatic conditions.

9. The water absorption, adsorption and film formation is highly depended on surface characteristics. When comparing polymer and ceramic surfaces, an increase in ambient relative humidity is not represented equally in both the EIS and the DC technique. Non-absorbing ceramic surfaces show a stronger effect on the DC signal, while humidity interactions of absorbing polymer surfaces are more represented in the EIS. The sole presence of humidity in the system is not directly transferable to an ECM risk. That is why it is important to understand humidity interactions in general, not only relying on one of the two techniques.

10. With regard to relating EIS and SIR values for ECM-criticality, sample layout is a key factor. Conventional DC SIR test patterns are designed with large interdigital anode-cathode regions in order to cover statistic dendrite occurrence. EIS measurements on such patterns however, will measure the overall mean condensate, masking the water bridge formation at one distinct spot that is needed for

ECM. For an accurate correlation of EIS and DC, appropriate specimen design is therefore crucial. Opposing anode-cathode region of narrow dimensions such as chip resistor footprints can serve as first reference. An accurate assessment of EIS values for ECM can then be used in the future for simulating condensation and water bridge formation leading to corrosion.

Overall, the findings verify that EIS is a promising method for humidity robustness evaluation for electronics. In relation with the DC tests, it is possible to establish a cause-effect relationship of water layer buildup and failure occurrence. In doing so, the EIS method delivers a detailed insight into the progressive steps of condensation and bridge formation, as well as onset of ECM by means of changes in resistive and capacitive system properties. Different PCBA design parameters as well as temperature and humidity conditions can thus be evaluated in terms of corrosion criticality. These results are a valuable contribution and the basis of the implementation of EIS as standardized method to assess electronics reliability in the future.

12. OUTLOOK

With the objective of using EIS for reliability assessment of electronics in climatic testing, the following issues should be addressed in the future.

Detailed studies with extended PCBA material and design parameters and climatic scenarios to evaluate full potential of EIS

The range of investigated variables should be extended in terms of various PCBA material and design parameters. This includes for example different solder paste variants that could be tested by EIS systematically to verify their climatic reliability. Also, the impact of surface temperature distribution on condensation and ECM should be further evaluated. In the PhD project, it was shown how this can be achieved for components that hamper condensation due to heat radiation. However, the reverse case can also be present on a PCBA. Components with large thermal masses can act as heat sinks and enforce condensation. This impact can be assessed likewise by EIS measurements. In the context of these investigations, a main emphasis should also be put on temporal effects. As the formation of thin water films on the PCBA surface is often transient, it is important to clarify how long a critical condition can be present until a dendrite grows. For that purpose, it is also advisable to perform measurements in different climatic scenarios, like conventional long time climatic tests (e.g. 85 °C and 85 %rH for 1000 hours). This way, through a hybrid combination of AC and DC testing, it can be clarified more extensively whether it is possible to define similar ECM-critical EIS threshold values, as has been done for condensing conditions. The possibility to use EIS for various testing scenarios is the prerequisite in order to, in the long run, employ the method as a validation tool in series testing or series production. Eventually, all these investigations should then contribute to the adaption of design and layout rules of electronic assemblies.

Alignment with different sensor systems and generation of a database for transfer of electrochemical data into simulation tools

In order to gain a deeper knowledge on relative humidity and temperature on the PCBA surface and its close proximity, it is necessary to perform more experiments with extensive sensor equipment. Incorporation of dew point sensors into the PCBA itself and relating the data with EIS measurement results can provide a better understanding of the local climate leading to condensation. Supporting the climate sensors, an automated evaluation with stereo camera systems should be pursued. A high-resolution in-situ recording, potentially in a 3D manner, can cover stages that are not in detail represented in T/rH-data, like droplet merging or bridge formation. However a simulation based solely on local temperature or humidity distribution does not serve the purpose of assessing corrosion criticality. Only in relation with DC/AC data, critical areas can be associated. The local and global information on the condensation along with EIS data

hinting to corrosion critical states can eventually be transferred into simulation parameters. Based on the holistic data, simulation models for humidity failures can be established.

Improvement of large-scale measurement technology

In comparison with measurement systems that are used for SIR testing, the measurement capabilities of AC technologies like EIS are significantly limited. Conventional DC systems used in industry's material release processes or platform testing are able to measure several hundred channels in parallel. This way, the systems are able to provide the statistically required analysis of empirical data. In contrast, EIS-systems are mostly available with several dozen measurement channels at maximum. The limited capabilities of EIS in terms of experiments' statistical statements discourage the use of this method for extensive evaluation for the time being. If the use of EIS is aimed to go beyond reaching an academic understanding of corrosion impact factors, it is necessary to develop measurement systems with similar large-scale capabilities like those available for SIR testing.

Evaluate EIS as a tool for an all-encompassing approach in PCBA reliability testing

The EIS method has a large sensitivity towards resistive and capacitive changes in a system and the possibility to represent these as physical models, for example in electrical equivalent circuits. In new test setups, the potential of recognizing and distinguishing three failure modes on different PCBA levels within one approach should be investigated:

1. On PCB: promising first results on humidity impact: absorbed humidity of PCB and condensation / surface water layer → risk for ECM was shown to be detectable by various EIS parameters
2. In solder joints: mechanical degradation (cracks etc.) → theoretically possible, no more cross sections necessary to prove failure mode
3. In components: Inner life of functioning components, for example internal wire breaks or degradation of polymer in electrolyte capacitor and consequent parameter drifts

Especially in product validation, this knowledge can be greatly beneficial. The possibility of having the whole product system represented by EIS variables (e.g. electrical equivalents) could serve the precise identification of a failure on a distinct product level.

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